CMOS Quad Channel UART (QUART)

PRELIMINARY

GENERAL DESCRIPTION

The EXAR Quad Universal Asynchronous Receiver and Transmitter (QUART) is a data communications device that provides four fully independent full duplex asynchronous communications channels in a single package. The QUART is designed for use in microprocessor based systems and may be used in a polled or interrupt driven environment.

The XR-82C684 offers a single IC solution for various microprocessor families. The 88 and 68 modes can be selected by tying SEL pin to VDD or VSS.

The QUART is fabricated using advanced two layer metal, with a high density EPI/CMOS process to provide high performance and low power consumption.

FEATURES

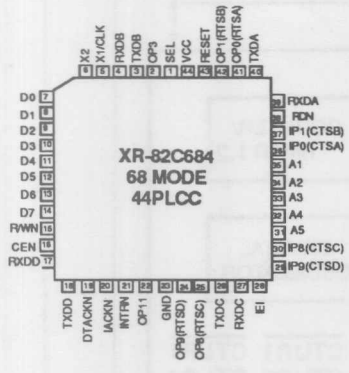
Four Full Duplex, Independent Channels, Asynchronous Receiver and Transmitter
Quadruple Receive and Transmit Buffer
Programmable Stop Bits in 1/16 Bit Increments
Pin Selectable 88 and 68 mode
Four Independent Internal Bit Rate Generators with more than 33 Bit Rates
Independent Bit Rate Selection for each Transmitter and Receiver
External Clock Capability
Normal, Autoecho, Local Loop Back and Remote Loopback Modes
Two Multifunction 16-Bit Counter/ Timer
Interrupt Output with Sixteen Maskable Interrupt Conditions
Prioritized Interrupt Vector Output on Acknowledge
Programmable Interrupt Daisy Chain
16 General Purpose Outputs
16 General Purpose Inputs with Eight Change of State Detectors on Inputs
Multidrop Mode Compatible with 8051 Nine-Bit Mode
On Chip Oscillator for Crystal
Stand-by Mode to Reduce Operating Power

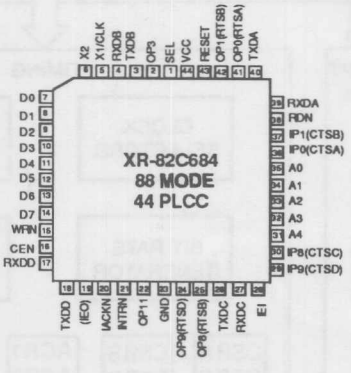
ABSOLUTE MAXIMUM RATINGS

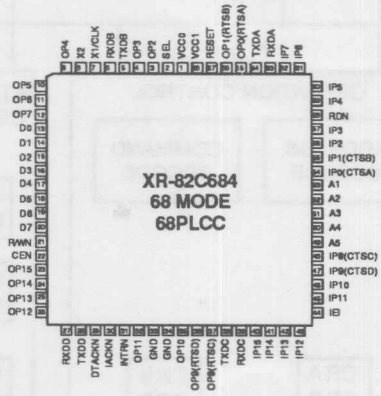
Storage Temperature	-65°C to150°C
All Voltages with respect to ground	-0.5 V to +7 V

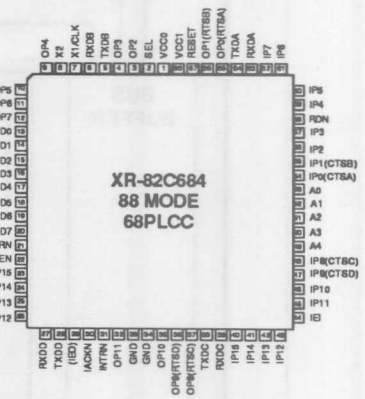
ORDERING INFORMATION

Part no.	Package	Operating Temperature
XR-82C684CJ/44	PLCC44 PIN	0° C to 70° C
XR-82C684J/44	PLCC44 PIN	-40° C to 85° C
XR-82C684CJ	PLCC68 PIN	0° C to 70° C
XR-82C684J	PLCC68 PIN	-40° C to 85° C









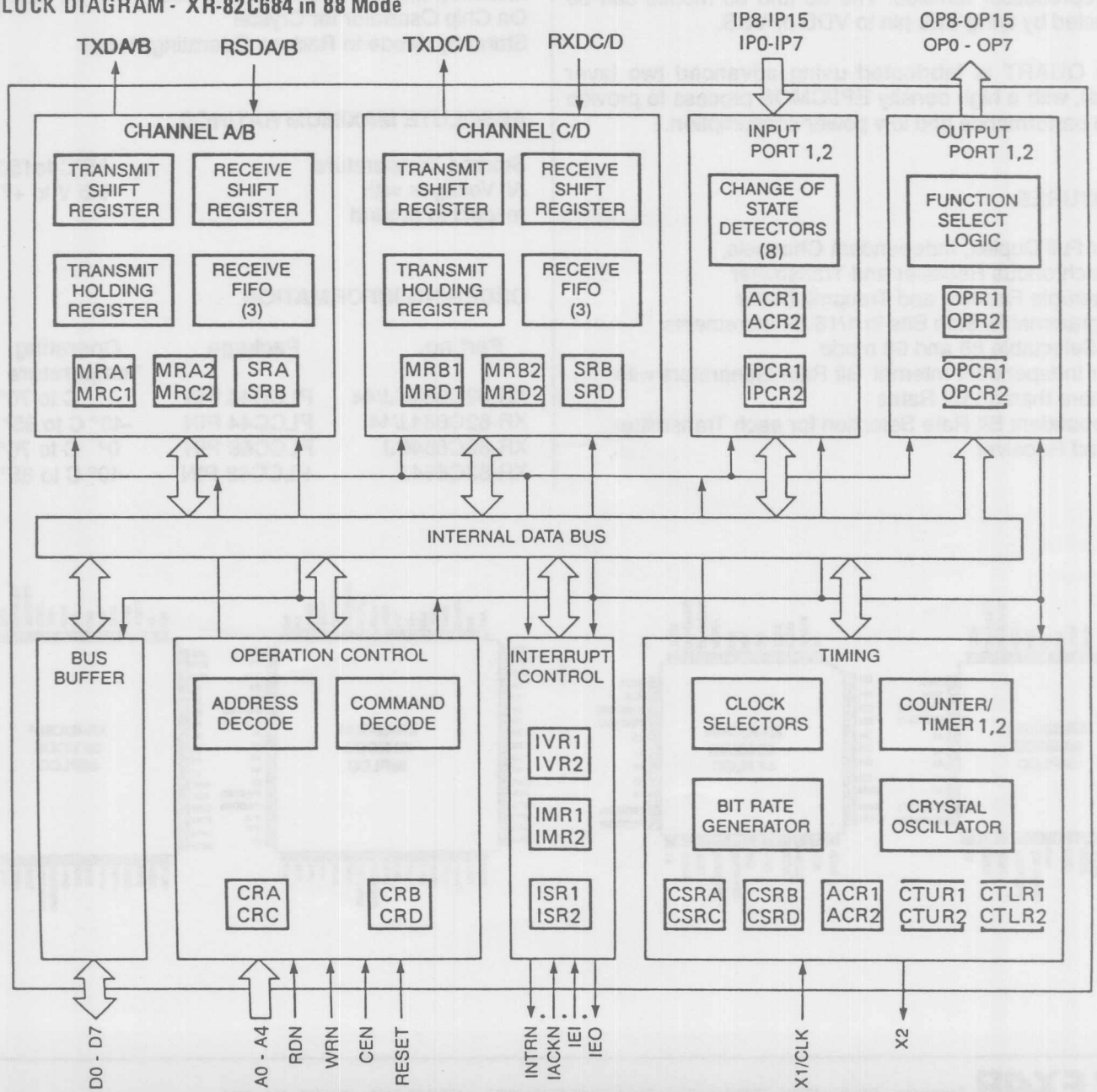
SYSTEM DESCRIPTION

Each channel of the QUART may be independently programmed for operating mode and data format. The operating speed of each receiver and transmitter may be selected from one of 33 internally generated fixed bit rates, from a clock derived from an internal counter/timer, or from an external 1x or 16x clock. The bit rate generator can operate directly from a crystal connected across two pins or from an external clock. The ability to independently program the operating speed of the receiver and transmitter of each channel makes the QUART attractive for split speed channel applications such as clustered terminal systems.

Receiver and transmitter data are quadruple-buffered in an on chip FIFO to minimize the risk of receiver or transmitter overrun and to reduce overhead in interrupt driven applications. The QUART also provides a flow control capability to inhibit transmission from a remote device when the buffer of the receiving QUART is full, thus preventing loss of data.

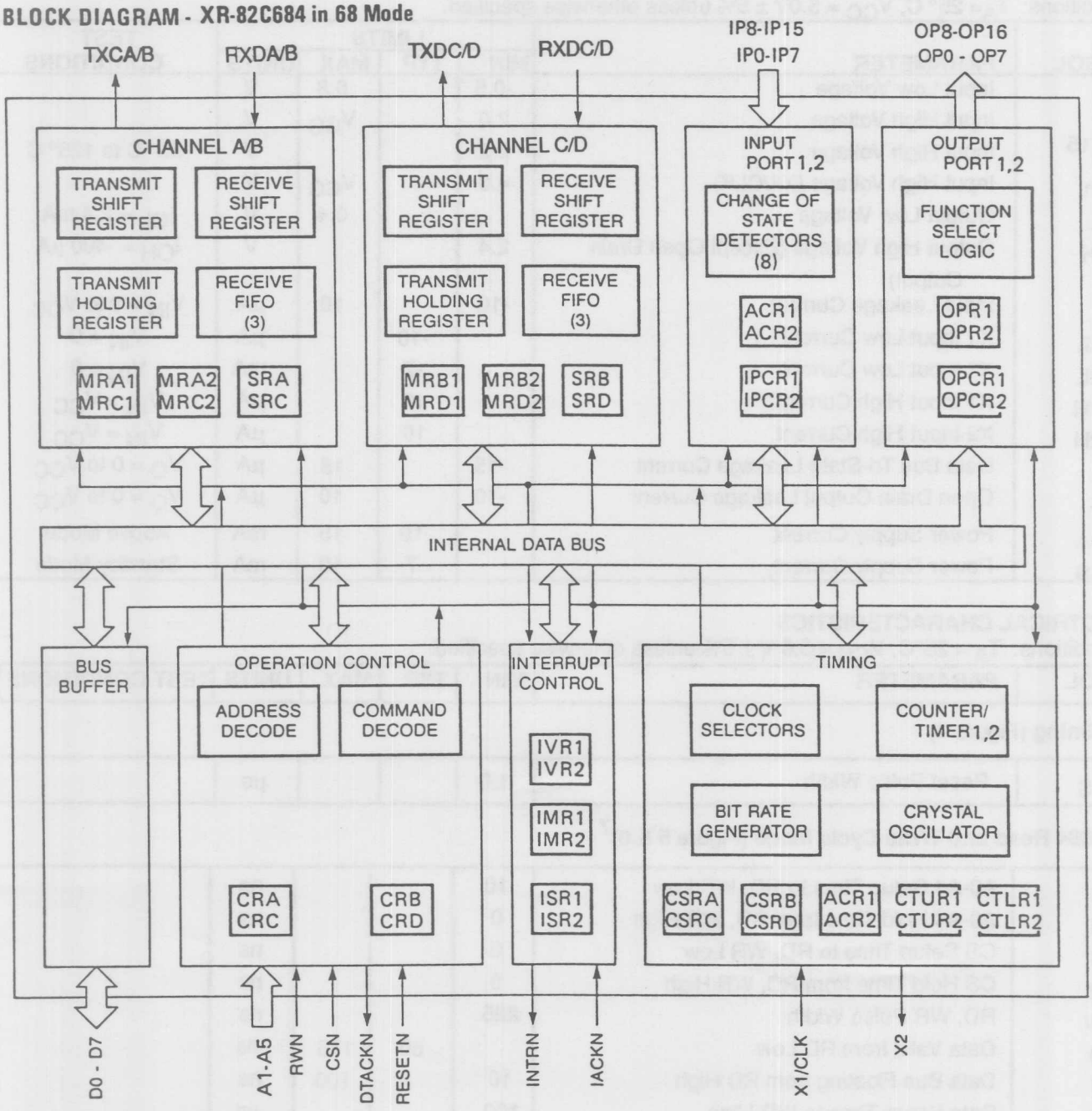
The QUART also provides two general purpose16 bit counter/timers (which may also be used as programmable bit rate generators), two multi-purpose input ports and two multi-purpose output ports.

BLOCK DIAGRAM - XR-82C684 in 88 Mode



* ALTERNATE FUNCTIONS FOR IP4 - IP6

BLOCK DIAGRAM - XR-82C684 in 68 Mode



DC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A= 25° C, V_{CC} = 5.0V ± 5% unless otherwise specified.

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{IH}[15]	Input High Voltage	2.2			V	-55° C to 125° C
V_{IH1}	Input High Voltage (X1/CLK)	4.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.4 mA
V_{OH}	Output High Voltage (Except Open Drain Output)	2.4			V	I_{OH} = -400 µA
I_{IL}	Input Leakage Current	-10		10	µA	V_{IN} = 0 to V_{CC}
I_{X1L}	X1 Input Low Current		-10		µA	V_{IN} = 0
I_{X2L}	X2 Input Low Current		-7		mA	V_{IN} = 0
I_{X1H}	X1 Input High Current		10		µA	V_{IN} = V_{CC}
I_{X2H}	X2 Input High Current		10		µA	V_{IN} = V_{CC}
I_{LL}	Data Bus Tri-State Leakage Current	-15		15	µA	V_O = 0 to V_{CC}
I_{OC}	Open Drain Output Leakage Current	-10		10	µA	V_O = 0 to V_{CC}
I_{CCA}	Power Supply Current		10	15	mA	Active Mode
I_{CCS}	Power Supply Current		7	10	mA	Standby Mode

AC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{CC} = 5.0 V ± 5% unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Reset Timing (Figure 4)						
t_{RES}	Reset Pulse Width	1.0			µs	
XR-82C684 Read and Write Cycle Mode (Figure 5 & 6)[7]						
t_{AS}	A0-A4 Setup Time to RD, WR Low	10			ns	
t_{AH}	A0-A4 Hold Time from RD, WR High	0			ns	
t_{CS}	CS Setup Time to RD, WR Low	0			ns	
t_{CH}	CS Hold Time from RD, WR High	0			ns	
t_{RW}	RD, WR Pulse Width	225			ns	
t_{DD}	Data Valid from RD Low		60	175	ns	
t_{DF}	Data Bus Floating from RD High	10		100	ns	
t_{DS}	Data Setup Time to WR High	100			ns	
t_{DH}	Data Hold Time from WR High	5			ns	
t_{RWD}	High Time Between Reads and/or Writes[8,9]	100			ns	
XR-82C684 Z-mode Interrupt Cycle Timing (Figure 6)						
t_{DIO}	IEO Delay Time from IEI			100	ns	
t_{IAS}	IACK Setup Time to RD Low	Note 10			ns	
t_{IAH}	IACK Hold Time from RD High	0			ns	
t_{EIS}	IEI Setup Time to RD Low	50			ns	
t_{EOD}	IEO Delay Time from INTR Low			100	ns	

XR-82C684 Read, Write and Interrupt Cycle Timing 68 Mode (Figure 7, 8, 9)

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{AS}	A1-A5 Setup Time to CS Low	10			ns	
t_{AH}	A1-A5 Hold Time from CS High	0			ns	
t_{RWS}	R/W Setup Time to CS Low	0			ns	
t_{RWH}	R/W Setup Time from CS High	0			ns	
t_{CSW}	CS High Pulse Width[9,11]	90			ns	
t_{CSD}	CS or IACK High from DTACK Low[12]	20			ns	
t_{DD}	Data Valid from CS or IACK Low			175	ns	
t_{DF}	Data Bus Floating from CS or IACK High	10		100	ns	
t_{DS}	Data Setup Time to CLK High	100			ns	
t_{DH}	Data Hold Time from CS High	0			ns	
t_{DAL}	DTACK Low from Read Data Valid	100			ns	
t_{DCR}	DTACK Low (read cycle) from CLK High			125	ns	
t_{DCW}	DTACK Low (write cycle) from CLK High			125	ns	
t_{DAH}	DTACK High from CS or IACK High			100	ns	
t_{DAT}	DTACK High Impedance from CS or IACK High			125	ns	
t_{CSC}	CS or IACK Setup Time to CLK High[13]	90			ns	

Port Timing 82C684 (Figure 10)[7]

t_{PS}	Port Input Setup Time to RD/CS Low	0			ns	
t_{PH}	Port Input Hold Time from RD/CS High	0			ns	
t_{PD}	Port Output Valid from WR/CS High			400	ns	

Interrupt Output Timing 82C684 (Figure11)

t_{IR}	INTR or OP3-OP7/OP10-OP15 When Used As Interrupts High from:					
	Clear of Interrupt Status Bits in ISR or IPCR			300	ns	
	Clear of Interrupt Mask in IMR			300	ns	

Clock Timing 82C684 (Figure 12)

t_{CLK}	X1/ CLK (External) High or Low Time	100			ns	
tCLK	X1/ CLK Crystal or External Frequency	2.0	3.684	7.372	MHz	
t_{CTC}	Counter/Timer External Clock High or Low Time (IP2 / IP10)	100			ns	
t_{CTC}	Counter/Timer External Clock Frequency	0		7.372	MHz	
t_{RTX}	RXC and TXC (External) High or Low Time[14]	220			ns	
fRTX	RXC and TXC (External) Frequency					
	16x	0		16.0	MHz	
	1x	0		1.0	MHz	

Transmitter Timing 82C684 (Figure 13)

t_{TXD}	TXD Output Delay - TXC (External) Low			350	ns	
t_{TCS}	TXD Output Delay - TXC (Internal) Output Low			150	ns	

Receiver Timing 82C684 (Figure 14)

t_{RXS}	RXD Data Setup Time to RXC External High	240			ns	
t_{RXH}	RXD Data Hold Time from RXC External High	200			ns	

PIN DESCRIPTIONS XR-82C684

MNEMONIC	TYPE	DESCRIPTION
D0-D7	I/O	**8-bit Bidirectional Three-state Data Bus.** Bit 0 is the LSB and bit 7 is the MSB. All transfers between the CPU and QUART take place over this bus. The bus is three-stated when the CS input is high, except during an IACK cycle or in the Z-mode.
A1-A5	I	**Address Inputs**. These inputs select the QUART registers or port for the current read/write operation.
CS	I	**Chip Select low**. The data bus is three-stated when CS is high. Transfers between the CPU and the QUART via D0-D7 are enabled when CS is low.
WR	I	**Write Strobe.** (88 mode) Active low. A low on this input while CS is also low writes the contents of the data bus into the addressed register.The transfer occurs on the rising edge of WR.
R/W	I	**Read / Write.** (68 mode) A high input while CS is low indicates a read cycle while a low input while CS is low indicates a write cycle.
RD	I	**Read Strobe**. (88 mode) Active low on this input while CS is also low places the contents of the addressed source on the data bus. The transfer begins on the falling edge of RD.
RESET	I	**Master Reset**. (Active high for 88 mode and Active low for 68 mode). Clears internal registers SRn, ISRn, IMRn, OPRn, OPCRn and initializes the IVRn to 0FH, stops the counter/timer, puts OP0-OP15 in the high state, and places both serial channels in the inactive state with the TXDA, TXDB, TXDC and TXDD outputs marking (high).
INTRN	O	**Interrupt Request**. Active low, open drain. INTRN is asserted upon the occurrence of one or more of the chip's maskable interrupting conditions.
IACK	I	**Interrupt Acknowledge.** (68 mode) Active low. Assertion of IACK indicates that the current bus cycle is an interrupt acknowledge cycle. If the QUART has an interrupt active, it responds by placing the interrupt vector on the data bus and asserting DTACK.
IEI	I	**Interrupt Enable Input.** (88 mode) Active high.
IEO	O	**Interrupt Enable Output**. (88 mode) Active high.
DTACK	O	**Data Transfer Acknowledge** (68 mode) Three state, active low. Assertion of DTACK indicates that data is present on the bus during a read or interrupt acknowledge cycle and that the data from the bus has been written into the addressed destination during a write cycle.
X1 / CLK	O	**Crystal Output or External Clock Input.** This pin is the connection for one side of the crystal and a capacitor to ground when the internal oscillator is used. If the oscillator is not used, an external clock signal must be supplied at this input.
X2	I	**Crystal Input.** Connection for other side of the crystal. If the oscillator is used, a capacitor must also be connected from this pin to ground. This pin must be left open if an external clock is supplied at X1 / CLK.

RXD-A RXD-B RXD-C RXD-D	I	**Receive Serial Data Inputs**. The least significant bit is received first. If external receiver clock is specified, the data is sampled on the rising edge of the clock.
TXD-A TXD-B TXD-C TXD-D	O	**Transmitter Serial Data Outputs**. The least significant bit is transmitted first. Held in the high (marking) state when the transmitter is idleordisabled and also when the channel operates in local loopback mode. If external transmitter clock is specified, the data is shifted out on the falling edge of the clock.
OP0	O	**Output 0.** Active low. Can be programmed as a general purpose output or as the channel A request-to-send output (RTS-A).
OP1	O	**Output 1.** Active low. Can be programmed as a general purpose output or as the channel B request-to-send output (RTS-B).
OP2	O	**Output 2.** Active low. Can be programmed as a general purpose output, the channel A transmitter 16x or 1x clock output, or the channel A receiver 1x clock output.
OP3	O	**Output 3**. Active low. Can be programmed as a general purpose output, the channel B transmitter 1x clock output, the channel B receiver 1x clock output, or an open drain counter/timer 1 ready output.
OP4	O	**Output 4**. Active low. Can be programmed as a general purpose output or as an open drain channel A RXRDY/FFULL output.
OP5	O	**Output 5**. Active low. Can be programmed as a general purpose output or as an open drain channel B RXRDY/FFULL output.
OP6	O	**Output 6.** Active low. Can be programmed as a general purpose output or as an open drain channel A TXRDY output.
OP7	O	**Output 7.** Active low. Can be programmed as a general purpose output or as an open drain channel B TXRDY output.
OP8	O	**Output 8**. Active low. Can be programmed as a general purpose output or as the channel C request-to-send output (RTS-C).
OP9	O	**Output 9.** Active low. Can be programmed as a general purpose output or as the channel D request-to-send output (RTS-D).
OP10	O	**Output 10.** Active low. Can be programmed as a general purpose output, the channel C transmitter 16x or 1x clock output, or the channel C receiver 1x clock output.
OP11	O	**Output 11.** Active low. Can be programmed as a general purpose output, the channel D transmitter 1x clock output, the channel D receiver 1x clock output, or an open drain counter/timer 2 ready output.
OP12	O	**Output 12**. Active low. Can be programmed as a general purpose output or as an open drain channel C RXRDY/FFULL output.
OP13	O	**Output 13**. Active low. Can be programmed as a general purpose output or as an open drain channel D RXRDY/FFULL output.
OP14	O	**Output 14.** Active low. Can be programmed as a general purpose output or as an open drain channel C TXRDY output.

OP15	O	**Output 15**. Active low. Can be programmed as a general purpose output or as an open drain channel D TXRDY output.
IP0	I	**Input 0.** General purpose input or CTS-A, the channel A active low clear- to-send input.
IP1	I	**Input 1**. General purpose input or CTS-B, the channel B active low clear to send input.
IP2	I	**Input 2**. General purpose input or the counter/timer 1 external clock input.
IP3	I	**Input 3.** General purpose input or the channel A transmitter external clock input.
IP4	I	**Input 4**. General purpose input or the channel A receiver external clock input.
IP5	I	**Input 5**. General purpose input or the channel B transmitter external clock input.
IP6	I	**Input 6.** General purpose input or the channel B receiver external clock input.
IP7	I	**Input 7**. General purpose input.
IP8	I	**Input 8**. General purpose input or CTS-C, the channel C active low clear-to-send input.
IP9	I	**Input 9**. General purpose input or CTS-D, the channel D active low clear-to-send input.
IP10	I	**Input 10**. General purpose input or the counter/timer 2 external clock input.
IP11	I	**Input 11.** General purpose input or the channel C transmitter external clock input.
IP12	I	**Input 12.** General purpose input or the channel C receiver external clock input.
IP13	I	**Input 13**. General purpose input or the channel D transmitter external clock input.
IP14	I	**Input 14.** General purpose input or the channel D receiver external clock input.
IP15	I	**Input 15.** General purpose input.
SEL	I	**Mode Select.** 88 mode can be selected by tying this pin to ground; connecting this pin to Vcc will select the 68 mode.
VCC	I	**+5 Volt Power Input**
GND	I	**Signal and Power Ground**

PRINCIPLES OF OPERATION

As illustrated in the block diagram, the QUART consists of the following major blocks:

Bus Buffer
Operation Control
Interrupt Control
Timing
Input Ports
Output Ports
Serial Communication Channels A, B, C and D

BUS BUFFER

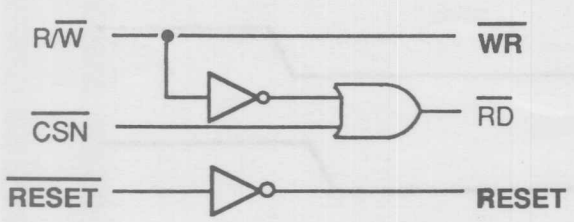
The data bus buffer provides the interface between the internal and external data buses. It is controlled by the operation control block to allow data transfers to take place between the host CPU and the QUART.

OPERATION CONTROL

The control logic receives operating commands from the CPU and generates proper signals to the various sections of the QUART. It contains address decoding and read/write circuits to permit communication with the microprocessor and internal registers, to set configuration commands and to monitor device status.

In the 68 mode (68000 Microprocessor Family), the QUART includes a data transfer acknowledge (DTACK) output which is asserted during data transfer cycle to verify that the requested operation has been completed. It indicates that the input data has been latched during a write cycle, that the requested data is on the data bus during a read cycle, or that the interrupt vector is on the data bus during an interrupt acknowledge cycle.

When using a 6800 family processor, the QUART should be used in the 88 mode. This can be readily achieved by implementing the minor external logic change as shown in the figure below:



Note: This is required for 6800 based microprocessors and is not necessary for 68000 based machines.

The addressing of the internal registers of the QUART is described in Table 1. The mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The MR1n pointer is set by a hardware reset or by 'reset pointer' command from command register (CRn bit4-7). Any read or write operation to the mode register while the pointer is pointing at MR1n switches the pointer to MR2n and remains there such that any subsequent accesses are always to MR2n unless the pointer is reset back to MR1n.

INTERRUPT CONTROL

An interrupt request output signal (INTRN) is provided which may be programmed to be asserted upon the occurrence of any of the following events:

Transmit Hold register A,B,C or D ready.
Receive Hold register A,B,C or D ready.
Receive FIFO A,B,C or D Full.
Start or End of received Break A,B,C or D
End of Counter/Timer count reached.
Change of State on input pins IP0,
IP1, IP2, IP3, IP8, IP9, IP10 or IP11

Associated with the interrupt system are the interrupt status register (ISRn), the interrupt mask register (IMRn), and the interrupt vector register (IVRn).The ISRn indicates the current state of all the potential interrupting conditions listed above. The IMRn may be programmed to select only certain of these conditions to assert the INTR output.

In the 88 mode, the QUART may be programmed to operate in two modes to accommodate different CPU interface requirements.

In the "I mode", which is the default mode, after a hardware reset, interrupt prioritization and interrupt vector generation, if required, are implemented using external hardware. In this mode, the on-chip interrupt vector register is not utilized and is available for use as an auxiliary read/write register for any purpose.

In the "Z mode", which is invoked via a command to command register B pin 21, 18 and 19 are designed as interrupt acknowledge (IACK), interrupt enable input (IEI) and interrupt enable output (IEO) respectively. IEI and IEO are the input and output of an interrupt daisy chain, as illustrated in Figure 1A. IEI high means that the QUART may generate an interrupt request.

A device with IEI high inhibits other devices by setting IEO low. Looking down the daisy chain; a device with IEI low must keep its IEO output low. This way it is possible to set up a predetermined priority chain in the system.

Sometime after the interrupt request, the CPU will respond with an interrupt acknowledge cycle, followed by a RD cycle (Figure 1B). The time between IACK and RD allows the daisy chain to stabilize. Also as long as IACK is asserted, the QUART is inhibited from issuing a new interrupt request. The device making the request sets its internal 'interrupt under service' (IUS) latch and places the vector from the IVR (Interrupt Vector Register) on the data bus. Upon completion, the CPU must issue a reset IUS latch command to the chip, which resets the latch and returns the daisy chain to its normal condition. In the 68 mode, the QUART has its interrupt request active and responds to the IACK input by placing the vector from the IVR on the data bus and asserting DTACK. Otherwise, it ignores IACK.

In either mode, outputs OP3-OP7 and OP11-OP15 can be programmed to provide separate open drain interrupt requests for transmitters A,B,C and D, receivers A,B,C and D, and the timer/counter 1, 2. See pin description.

TIMING

The timing block as illustrated in Figure 2 contains a crystal oscillator, a bit rate generator (BRG), a programmable 16-bit counter/timer (C/T), and four clock selectors.

The crystal oscillator operates from a parallel crystal connected between the X1/CLK and X2 pins. A crystal frequency of 3.6864 or 7.3728 MHz is required for generation of standard bit rates by the bit rate generator (see Table 3). A crystal clock or an external TTL clock signal on the X1/CLK pin can be used either directly or it can be divided by two before being used to generate the internal system clock. If an external clock is available, it may be connected to X1/CLK, with X2 left open.

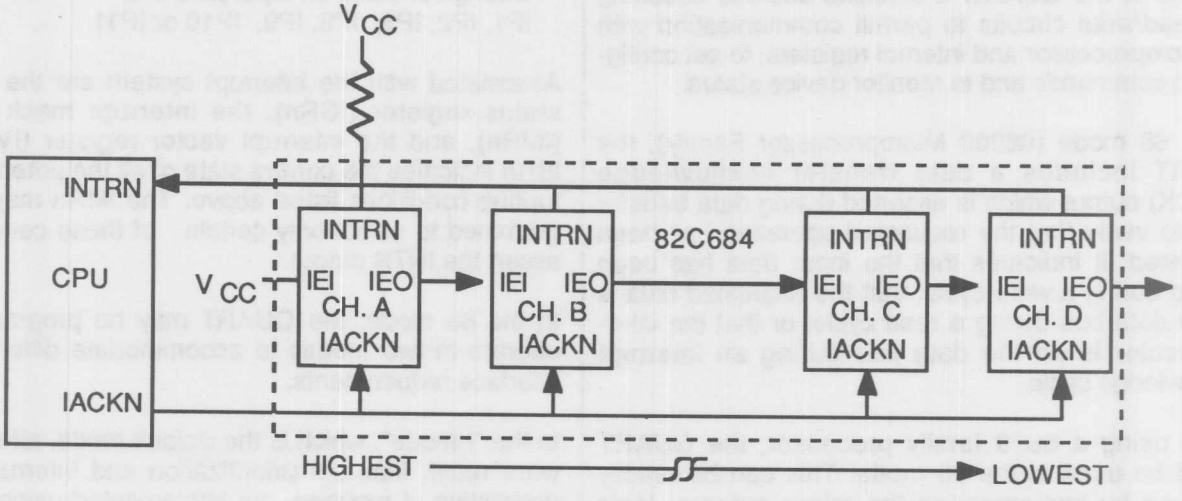


Figure 1A. Daisy Channel Interrupt Block Diagram

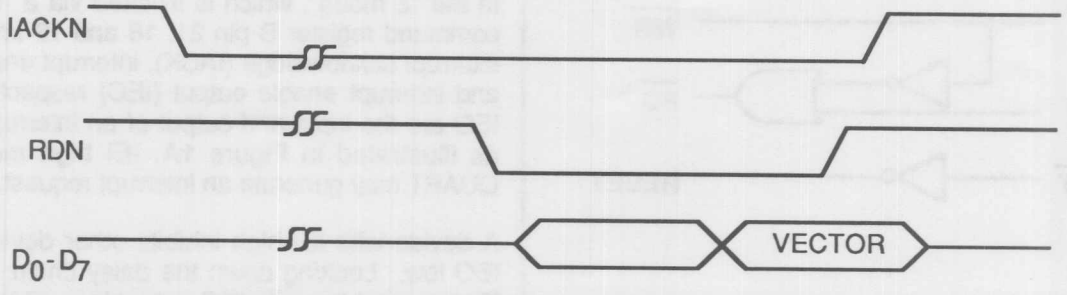


Figure 1B. Daisy Chained Interrupt Timing

The output of the oscillator is used by the BRG, the C/T and other internal circuits. This requires that a clock within the specified limits always be supplied to the QUART.

Bit Rate Generator

The BRG uses the crystal oscillator or external clock as an input and generates the clock for 33 commonly used data communications bit rates ranging from 50 to 230.4K bits per second. The actual clock frequencies output from the BRG are at 16 times these rates. The counter/timer can also be used as a programmable bit rate generator to produce a 16x clock for any bit rate not provided by the BRG. The four clock select multiplexers/per channel allow each receiver and transmitter to independently select its operating frequency as one of the outputs from the BRG, the output of the counter/timer, or an external clock. (See Input Port Selection in the Pin Description Table, page 8)

Counter /Timer

Each C/T is a programmable 16-bit down-counter which can use one of several timing sources as their input. The C/T outputs are available to the clock selectors for use as a programmable bit rate for any receiver or transmitter (note that counter/timer 1 is used for A/B receiver and transmitter, counter/timer 2 is used for C/D receiver and transmitter), each can be programmed to generate an interrupt each time it reaches its terminal count of OOOOH, and can also be programmed as an output at OP3 and OP11.

In the timer mode, the C/T acts as a programmable divider and generates a square wave whose period is twice the value (in clock periods) of the contents of the counter/timer registers CTUR and CTLR. The contents of these registers may be changed at any time, but will only begin to take effect at the next half cycle of the square wave. The C/T begins operation using the values in CTUR/CTLR upon receipt of a 'start counter' command (see Table 1).

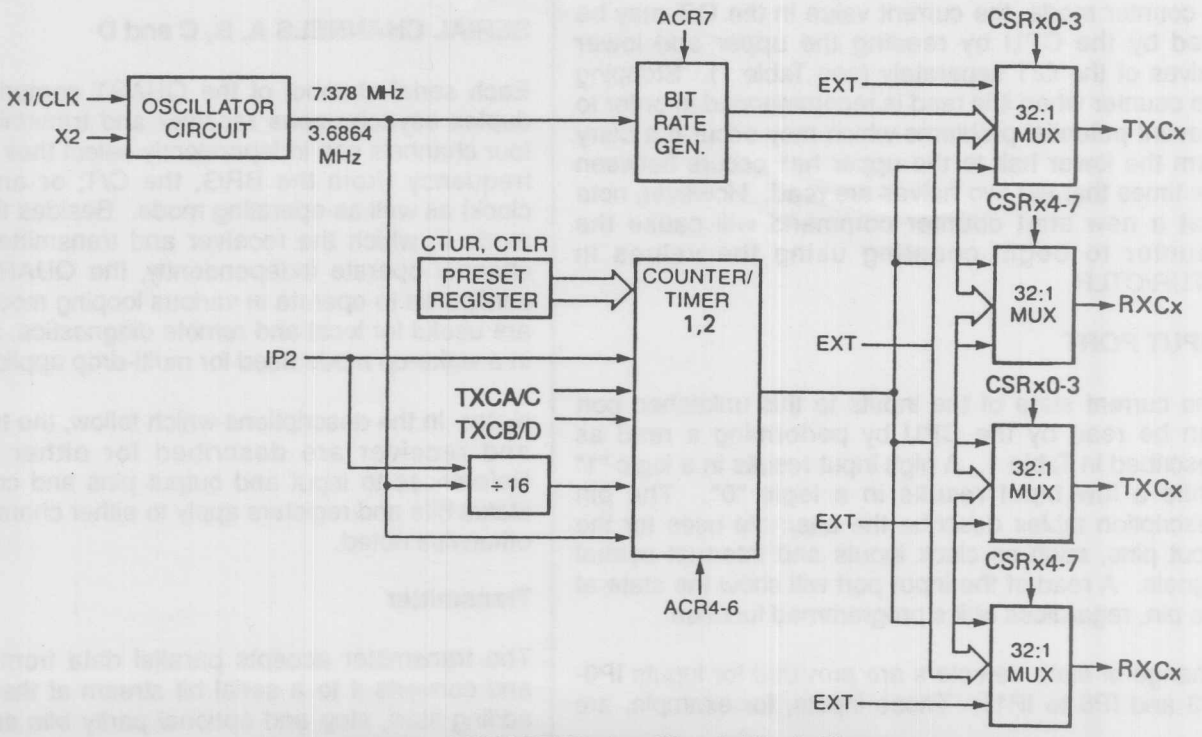


Figure 2. Half of QUART Timing Circuit Block Diagram

The C/T then runs continuously. A subsequent 'start counter' command causes the C/T to terminate the current timing cycle and begin a new timing cycle using the current values in CTUR and CTLR. The counter ready status bit (ISRn) is set once each cycle of the square wave. This allows use of the C/T as a periodic interrupt generator if the condition is programmed to generate an interrupt via the interrupt mask register. The status bit can be reset by issuing a 'stop counter' command (see Table 1). In this mode, however, the command does not actually stop the C/T. The generated square wave is output on OP3 or OP11 if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses written into CTUR/CTLR, beginning at the receipt of a 'start counter' command. The counter ready status bit (ISR [3]) is set upon reaching the count of OOOOH. The C/T will continue to count past this (with the next count being FFFFH) until it is stopped by the CPU via a 'stop counter' command. If OP3 or OP11 is programmed to be the output of the C/T, the output remains high until the terminal count is reached, at which time the output goes low. It then returns to the high state and ISR[3] is cleared when the counter is stopped. A 'start counter' command while the counter is running restarts the counter with the values in CTUR/CTLR. The CPU may change CTUR or CTLR at any time but the new count takes effect only on the next start counter command. If new values are not programmed, the previous values are preserved and used for the next cycle.

In counter mode, the current value in the C/T may be read by the CPU by reading the upper and lower halves of the C/T separately (see Table 1). Stopping the counter when it is read is recommended in order to prevent potential problems which may occur if a carry form the lower half to the upper half occurs between the times that the two halves are read. However, note that a new start counter command will cause the counter to begin counting using the values in CTUR/CTLR.

INPUT PORT

The current state of the inputs to this unlatched port can be read by the CPU by performing a read as described in Table 1. A high input results in a logic "1" while a low input results in a logic "0". The pin description tables describe the alternate uses for the input pins, such as clock inputs and interrupt control signals. A read of the input port will show the state at the pin, regardless of it s programmed function.

Change of state detectors are provided for inputs IP0-IP3 and IP8 to IP11. These inputs, for example, are sampled by the 38.4 kHz output of the BRG (2.4 Kbps x 16). A high-to-low or low-to-high transition at these inputs lasting at least two clock periods (approximately 50 µs) will guarantee that the corresponding bit in the input port change register (IPCR) will be set, although it may be set by a change of state as short as 25 µs. The status bits in the IPCR are cleared when the register is read by the CPU. Any change of state can also be programmed to generate an interrupt.

OUTPUT PORT

The output ports can be used as a general purpose output or can be used to output timing and status signals by appropriately programming of the mode registers (MR1A-D, MR2A-D) and also the output port configuration registers. When used to output status signals the pins are open drain, which allows their use in a wire OR interrupt scheme.

When used as a general purpose output port, the outputs are the complements of the output port register (OPR). $OPR_{(n)}$ = 1 results in $OP_{(n)}$ low while $OPR_{(n)}$ = 0 results in $OP_{(n)}$ high. Bits of OPR can be set and reset individually. A bit is set by the address-triggered 'set output port bits' command (see Table 1) with the accompanying data specifying the bits to be set (1 = set, 0 = no change). A bit is reset by the address-triggered 'reset output port bits' command (see Table 1) with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

SERIAL CHANNELS A, B, C and D

Each serial channel of the QUART comprises a full duplex asynchronous receiver and transmitter. The four channels can independently select their operating frequency (from the BRG, the C/T, or an external clock) as well as operating mode. Besides the normal mode in which the receiver and transmitter of each channel operate independently, the QUART can be configured to operate in various looping modes, which are useful for local and remote diagnostics, as well as in a wake-up mode used for multi-drop applications.

Note: In the descriptions which follow, the transmitter and receiver are described for either channel. References to input and output pins and control and status bits and registers apply to either channel unless otherwise noted.

Transmitter

The transmitter accepts parallel data from the CPU and converts it to a serial bit stream at the TXD pin, adding start, stop and optional parity bits as required by the asynchronous protocol.

The QUART is conditioned to transmit data when the transmitter is enabled via the command register. It indicates that it is ready to accept a character from the CPU for serialization by setting the TXRDY bit in the status register. This condition can be programmed to assert an interrupt request via the INTRN output and can also be programmed to assert the OP6/14 output (channel A/C) or the OP7/15 output (channel B/D). These conditions are negated when the CPU loads a character into the transmit holding register (THR). Data is transferred form the THR to the transmit shift register (TSR) immediately if the TSR is idle or when it completes serialization of the previous character. The TXRDY condition is then asserted again. Thus, one full character time of buffering is provided. Note that the THR will not accept characters while the transmitter is disabled.

The transmitter sends a start bit followed by the programmed number of data bits (least significant bit first), an optional parity bit, and the programmed number of stop bits and begins transmission of the next character if one has been loaded into the THR. Otherwise, the TXD output will remain high and the TXEMT status bit will be set following the transmission of the stop bits. Transmission resumes and the TXEMT status bit is cleared when the CPU loads a new character into the THR. The transmitter can be forced to send a continuous low at TXD by invoking a 'send break' command.

If the transmitter is disabled, it continues operating until the character currently being serialized, and any in the THR, are completely sent out. The transmitter can be reset by a software command. In this case, operation ceases immediately and the transmitter must be re-enabled before resuming operation.

Setting MR2n[4] of the appropriate channel programs its transmitter to begin transmission of a character only if the channels clear-to-send input pin (IP0 for channel A, IP1 for channel B, IP8 for channel C and IP9 for channel D) is low. If CTSN goes high in the middle of a transmission, the transmission of the current character is completed but TXD remains high and the next character will not be sent until CTSN is low again. Setting MR2[5] of the appropriate channel programs the transmitter to automatically deactivate its request-to-send output pin (OP0 for channel A, OP1 for channel B, OP8 for channel C and OP9 for channel D). If so programmed, and the transmitter has been disabled, the RTSN output will be negated one bit time after the characters in the TSR and THR (if any) are completely sent.

Receiver

The receiver accepts serial data at its RXD pin, checks for a proper start bit, converts the serial input to parallel form, checks the parity bit (if parity is specified), checks for presence of a stop bit, performs several other tests on the received data, and sends the assembled character to the CPU.

Each receiver is conditioned to receive data when it is enabled via the command register. It looks for a high to low (mark to space) transition indicating a start bit at the RXD input. If a transition is detected, the state of RXD is sampled each 16x clock for 7 1/2 clocks (16x clock mode) or at the next rising edge of the bit time clock (1x clock mode). If RXD is detected high at these sample times, the start bit is invalid and the search for a start bit begins again. If RXD remains low, a valid start bit is assumed and the receiver continues to sample the data at one bit time intervals, at the theoretical center of the bit , until the programmed number of data bits (LSB first), the parity bit (if any), and one stop bit have been assembled. The data is then transferred to the receive holding register (RHR) with the most significant unused bits set to zero. The status conditions (parity error, framing error, overrun error, and break received) are set to indicate to the CPU that a character is available to be read. Setting of RXRDY can be programmed to generate an interrupt request via INTRN and to assert OP4 (channel A), OP5 (channel B), OP12 (channel C) and OP13 (channel D).

After the stop bit position is sampled, the receiver will immediately begin to look for the start bit of the next character. However, if a non-zero character was received without a stop bit time after sampling of the stop bit, the receiver operates as if a new start bit transition had been detected at that point (half a bit time after the sampling of the stop bit).

If a break is received (an all zeroes character including the first stop bit), only a single character consisting of all zeroes will be loaded into the FIFO and the break received status bit will be set, no matter how long the break condition persists. RXD must return to a high condition for at least half a bit time before the search for a new start bit begins again.

The RHR consists of a first-in-first-out (FIFO) stack with a capacity of three characters. Data is transferred from the receive shift register into the topmost empty position in the FIFO. RXRDY is set whenever one or more characters are in the FIFO, and the FFULL status bit is set if the FIFO is filled with data. Either of these bits can be selected to assert an interrupt. A read of the RHR outputs the data at the top of the FIFO and any remaining characters are pushed up, thus freeing a FIFO position for new data.

In addition to the data word, three status bits are appended to each character position in the FIFO. These are parity error, framing error, and received break. Status can be provided in two ways, as programmed by MR1[5] in the channels mode register. In the 'character' mode, status is provided on a character by character basis: the status applies only to the character at the top of the FIFO. In the block mode, these three bits in the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode, reading the status register does not affect the FIFO. The FIFO is popped only when the RHR is read. Therefore, the status register should be read prior to reading the RHR. Also note that PE, FE and received break status register is asserted.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If a new start bit is detected while this condition exists, the character previously in the shift register is lost and the overrun error status bit is set. The contents of the FIFO are not affected when this occurs.

If the receiver is disabled, the contents of the FIFO are maintained and can be read by the CPU. Resetting the receiver initializes the FIFO pointers and clears the status bits immediately. In either case, any character currently being assembled is lost and operation does not resume until the receiver is re-enabled.

Setting MR[7] of the appropriate channel programs the receiver to automatically control de-activation of the request-to-send output (OP0 for channel A, OP1 for channel B). If so programmed, RTSN will be negated when a valid start bit is received while the FIFO is full, and will automatically be re-asserted when a FIFO position becomes available for that character. This feature can be used to prevent an overrun in the receiver by connecting the RTSN output to the CTSN input of the transmitting device.

Multidrop (8051 9-bit) Mode

Each serial channel of the QUART can be configured to operate in a wake-up mode useful for multidrop or multiprocessor applications. This mode is compatible with the serial 'Nine-bit Mode' of 8051-family microcomputers. In this mode of operation a master station, connected to a maximum of 256 slave station, transmit an address character followed by a block of data characters targeted for the addressed slave station. The slave stations normally have their receivers disabled. However, in this mode, the slave receivers monitor the incoming data stream and wake up the CPU (by asserting RXRDY) when any address character is detected. The slave station CPU then compares the received address to its own assigned address and enables the receiver, if it wishes, to receive the subsequent block of data, or leaves the receiver disabled if it does not. Upon completion of reception of the block of data, the receiver is disabled to re-initiate the process.

The multidrop mode is selected by programming MR[4:3] of the channel to '11'. In this mode, a transmitted character consists of a start bit, the programmed number of data bits, and address/data flag bit (A/D), and the programmed number of stop bits. A/D = 0 indicates that the character is data, while A/D = 1 identifies it as an address. The CPU controls the state of A/D in the transmitted character by programming MR1[2] of the channel prior to loading the data bits into the THR. MR1[2] = 0 results in A/D = 0 and MR1[2] =1 results in A/D =1.

In the multidrop mode, the receiver continuously looks at RXD whether enabled or not. When disabled, it loads a character into the RHR and sets RXRDY if its A/D bit is one (address flag) but discards the character if its A/D bit is zero (data flag). If the receiver is enabled, all characters received are transferred to the RHR. In either case, the received data bits are loaded into the RHR while the A/D bit is loaded into SR[5], the status register position normally used for parity error. Framing error, overrun error, and break detect status bits operate normally.

Standby Mode

The QUART may be placed in a standby mode to conserve power when its operation is not required. Upon reset, the QUART will be in the 'active operation' mode. A 'set standby mode' command issued via the channel A command register disables all clocks on the device except for the crystal oscillator, which significantly reduces the operating current. In this mode the only functions which will operate correctly are reading the input port, writing the output port and the 'set active mode' command. The latter, also invoked via the channel A command register, restores the device to normal operation within 25 µs. Resetting the transmitters and receivers and writing 00H into the interrupt mask register before going into the standby mode is recommended to prevent any spurious interrupts from being generated. The chip should be reprogrammed after the 'set active mode' command since register contents are not guaranteed to remain stable during the standby mode. Active operation can also be restored via hardware reset.

TABLE 1. QUART PORT AND REGISTER ADDRESSING

Address (HEX)	Reading From The Registers	Writing To The Registers
0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
1	Status Register A (SRA)	Clock Select Register A (CSRA)
2	Masked Interrupt Status Register 1(MISRA)	Command Register A (CRA)
3	Rx Holding Register A (RHRA)	Tx Holding Register A (THRA)
4	Input Port Change Register 1 (IPCR1)	Auxiliary Control Register A (ACRA)
5	Interrupt Status Register 1 (ISR1)	Interrupt Mask Register 1 (IMR1)
6	Counter/Timer 1 Upper byte (CTU1)	Counter/Timer 1 Upper Register (CTUR1)
7	Counter/Timer 1 Lower byte (CTL1)	Counter/Timer 1 Lower Register (CTLR1)
8	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
9	Status Register B (SRB)	Clock Select Register B (CSRB)
A	RESERVED	Command Register B (CRB)
B	Rx Holding Register B (RHRB)	Tx Holding Register B (THRB)
C	Interrupt Vector Register A (IVR1)	Interrupt Vector Register 1 (IVR1)
D	Input Port A (IP1)	Output Port Configuration Register 1 (OP0-OP7), (OPCRA)
E	Start Counter/Timer 1 (SCC1)	Set Output Port Bits Command 1 (SOPBC1)
F	Stop Counter/Timer Command 1 (STC1)	Reset Output Port Bits Command 1 (ROPBC1)
10	Mode Register C (MR1C, MR2C)	Mode Register C (MR1C, MR2C)
11	Status Register C (SRC)	Clock Select Register C (CSRC)
12	Masked Interrupt Status Register 2(MILSRB)	Command Register C (CRC)
13	Rx Holding Register C (RHRC)	Tx Holding Register C (THRC)
14	Input Port Change Register 2 (IPCR2)	Auxiliary Control Register B (ACRB)
15	Interrupt Status Register 2 (ISR2)	Interrupt Mask Register B (IMR2)
16	Counter/Timer 2 Upper byte (CTU2)	Counter/Timer 2 Upper Register (CTUR2)
17	Counter/Timer 2 Lower byte (CTL2)	Counter/Timer 2 Lower Register (CTLR2)
18	Mode Register D (MR1D, MR2D)	Mode Register D (MR1D, MR2D)
19	Status Register D (SRD)	Clock Select Register D (CSRD)
1A	RESERVED	Command Register D (CRD)
1B	Rx Holding Register D (RHRD)	Tx Holding Register D (THRD)
1C	Interrupt Vector Register B (IVR2)	Interrupt Vector Register 2 (IVR2)
1D	Input Port B (IP2)	Output Port Configuration Register 2 (OP8-OP15), (OPCRB)
1E	Start Counter/Timer 2 (SCC2)	Set Output Port Bits Command 2 (SOPBC2)
1F	Stop Counter/Timer Command 2 (STC2)	Reset Output Port Bits Command 2 (ROPBC2)

TABLE 2. REGISTER BIT FORMATS

MR1A-D

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Rx RTS Control	Rx Int Select	Error Mode	Parity Mode		Parity Type	Bits Per Char.	
0 = no 1 = yes	0 = RXRDY 1 = FFULL	0 = char 1 = block	00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multi-drop Mode		0 = even 1 = odd	00 = 5 01 = 6 10 = 7 11 = 8	

MR2A-D

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Channel Mode		Tx RTS Control	CTS Enable Tx	Stop Bit Length*			
00 = Normal 01 = Auto Echo 10 = Local Loop 11 = Remote Loop		0 = no 1 = yes	0 = no 1 = yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

*Add 0.5 to values shown for 0-7 if channel is programmed for 5 bits/character.

CSRA-D

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Receiver Clock Select				Transmitter Clock Select			
See Table 3				See Table 3			

CRA-D

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Miscellaneous Commands				Disable Tx	Enable Tx	Disable Rx	Enable Rx
See Text				0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes

SRA-D

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Received Break	Framing Error	Parity Error	Overrun Error	TXEMT	TXRDY	FFULL	RXRDY
0 = no 1 = yes *	0 = no 1 = yes *	0 = no 1 = yes *	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes

*These status bits are appended to the corresponding data character in the receive FIFO. A read of the status register provides these bits (7:5) from the top of the FIFO together with bits 4:0. These bits are cleared by a 'reset error status' command. In character mode they are discarded when the corresponding data character is read from the FIFO.

OPCR1,2

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OP7/OP15	OP6/OP14	OP5/OP13	OP4/OP12	OP3/OP11		OP2/OP10	
0 = OPR[7/15] 1=TXRDYB/D	0 = OPR[6/14] 1=TXRDYA/C	0 = OPR[5/13] 1 = RXRDY/ FFULLB/D	0 = OPR[4/12] 1 = RXRDY/ FFULLA/C	00 = OPR[3/11] 01 = C/T Output 10 = TxCB/D(1X) 11 = RxCB/D(1X)		00 = OPR[2/10] 01 = TXCA/C(16X) 10 = TXCA/C(1X) 11 = RXCA/C(1X)	

ACR1,2

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BRG Set Select	Counter/Timer Mode and Source			Delta IP3/IP11	Delta IP2/IP10	Delta IP1/IP9	Delta IP0/IP8 Int
0 = Set1 1 = Set2	See Table 6			0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

TABLE 2. REGISTER BIT FORMATS (continued)

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IPCR1,2	Delta IP3/IP11	Delta IP2/IP10	Delta IP1/IP9	Delta IP0/IP8	IP3 IP11	IP2 IP10	IP1 IP9	IP0 IP8
	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
ISR1,2	Input Port Change 1, 2	Delta Break B/D	RXRDY/ FFULLB/D	TXRDYB/D	Counter Ready 1, 2	Delta Break A/C	RXRDY/ FFULLA/C	TXRDYA/C
	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IMR1,2	Input Port Change Int 1, 2	Delta Break B/D Int	RXRDY/ FFULLB/D Int	TXRDYB/D Int	Counter Ready Int 1, 2	Delta Break A/C Int	RXRDY/ FFULLA/C Int	TXRDYA/C Int
	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CTU1,2	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]
CTUR1,2								

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CTL1,2	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]
CTLR1,2								

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IVR1,2	IVR[7]	IVR[6]	IVR[5]	IVR[4]	IVR[3]	IVR[2]	IVR[1]	IVR[0]

PROGRAMMING

Operation of the QUART is programmed by writing control words into the appropriate registers, while operational feedback is provided by status registers which can be read by the CPU. Register addressing is shown in Table 1.

A hardware reset clears the contents of SRA, SRB, IMR, ISR, OPR and OPCR and initializes the IVR to 0FH. During operation, care should be exercised if the contents of control registers are to be changed, since certain changes may result in improper operation. For example, changing the number of bits per character while data is being received may result in reception of an erroneous character. In general, changes to registers which control receiver or transmitter operation should be made only while the transmitter or receiver are disabled, and certain changes to the ACR should be made only when the C/T is stopped.

Mode, command, clock select, and status registers are duplicated for each channel to provide totally independent operation. Table 2 illustrates the bit assignments for each register.

Note: In the descriptions which follow, registers which are duplicated for each channel are described generically. References to input and output pins and control and status bits and registers apply to each channel unless otherwise noted.

MODE REGISTER 1 (Channels A - D)

MR1 for each channel is accessed when the channel's MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command invoked via the channel's command register. After reading or writing MR1, the pointer will point to MR2.

MR1(7) - Receiver Request-to-Send Control

This bit controls the negation of the RTSN output (OP0 for channel A, OP1 for channel B, OP8 for channel C and OP9 for channel D) by the receiver. RTSN is normally asserted by setting the respective output bit (OP 1/2/8/9 for channels A/B/C/D), and negated by resetting the same bit. MR1(7) = 1 causes RTSN to be negated automatically upon receipt of a valid start bit if the channel's FIFO is full and to be re-asserted again when an empty FIFO position becomes available. This flow control feature can be used to prevent overrun of the receiver by using the RTSN output to control transmission of characters to the QUART.

MR1(6) - Receiver Interrupt Select

This bit selects either the RXRDY status bit or the FFULL status bit of the channel to be used for CPU interrupts. It also causes the selected bit to be output on OP4 channel A, OP5 channel B, OP12 channel C or OP13 channel D.

MR1(5) - Error Mode Select

This bit controls the operation of the three FIFO status bits (PE, FE, received break) for the channel. In the character mode these status bits apply only to the character currently at the top of the FIFO. In the block mode these bits are the cumulative logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command for the channel was issued.

MR1(4:3) - Parity Mode Select

If 'with parity' or 'force parity' operation is programmed, a parity bit is added to the transmitted characters and the receiver performs a parity check on received characters. See OPERATION section for description of multidrop mode operation.

MR1(2) - Parity Type Select

This bit selects odd or even parity if 'with parity' mode is programmed and the state of the forced parity bit if the 'force parity' mode is programmed. In the multidrop mode it selects the state of the A/D flag bit. This bit has no effect if 'no parity' mode is programmed.

MR1(1:0) - Bits per Character Select

Selects the number of bits to be transmitted and received in the data field of the character. This does not include start, parity and stop bits

MODE REGISTER 2 (Channels A-D)

MR2 for each channel is accessed when the channel's MR pointer points to MR2, which occurs after any access to the channel's MR1. Reading or writing MR2 does not change the pointer.

MR2(7:6) - Channel Mode Select

Each channel can operate in one of four modes. MR2(7:6) = 00 in the normal mode where the receiver and transmitter operate independently.

MR2(7:6) = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions apply while in this mode:

1. Received data is transmitted on the channel's TXD output.

2. The receiver must be enabled but the transmitter need not be enabled.

3. The channel's TXRDY and TXEMT status bits are inactive.

4. The received parity is checked but is not regenerated for transmission. Thus, transmitted parity is as received.

5. Character framing is checked but the stop bits are transmitted as received.

6. A received break is echoed as received until the next valid start bit is detected.

7. CPU to receiver communications operate normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured.

The first is the local loopback mode, selected by MR2(7:6) = 10. In this mode:

1. The transmitter output is internally connected to the receiver input.

2. The transmit clock is used for the receiver.

3. The channel's TXD output is held marking (high).

4. The channel's RXD input is ignored.

5. The transmitter is enabled, but the receiver need not be enabled.

6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2(7:6) = 11. In this mode:

1. Received data is transmitted on the channel's TXD output.

2. Received data is not sent to the CPU and the error status conditions are not checked.

3. Parity and framing (stop bits) are transmitted as received.

4. The receiver must be enabled.

5. A received break is echoed as received until the next valid start bit is detected.

Care must be taken when switching into and out of the various modes. The selected mode will be activated immediately after it is programmed even if this occurs in the middle of transmitting or receiving a character. An exception to this is switching out of autoecho or remote loopback modes: if this deselection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RXRDY), and the transmitter is enabled, the transmitter will remain in autoecho or remote loopback mode until one entire stop bit has been transmitted.

MR2(5) - Transmitter Request-to-Send Control

This bit controls the negation of the RTSN output (OP0 for channel A, OP1 for channel B, OP8 for channel C and OP9 for channel D) by the transmitter. RTSN is normally asserted by setting the respective output port bits (OP1/2/8/9 for channels A/B/C/D) and negated by resetting the same bit. MR2(5) = 1 causes OP1/2/8 or 9) to be reset automatically one bit time after the characters in the channel's transmit shift register and THR, if any, are completely transmitted, including the programmed number of stop bit, if the transmitter has been disabled. This feature can be used to automatically negate RTSN at the conclusion of a message as follows:

1. Program auto-reset mode (MR2[5] =1).

2. Enable transmitter and assert the channel's RTSN output by setting the appropriate bit in the output port register.

3. Send message.

4. Disable the transmitter after the last character of the message is loaded into the THR.

MR2(4) - Clear-to-Send Control

If this bit is a 0, the channels CTSN input (IP0 for channel A, IP1 for channel B, IP8 for channel C and IP9 for channel D) has no effect on the transmitter. If the bit is a 1, the transmitter checks the state of its CTSN each time it is ready to send a character. If CTSN is low, the character is transmitted. If CTSN is high, TXD remains in the marking state and the transmission of the next character is delayed until CTSN goes low. Changes in CTSN while a character is being serialized do not affect transmission of that character.

MR2(3:0) - Stop Bit Length

This field programs the duration of the stop bit appended to each transmitted character. Stop bit durations of 9/16 to 1 bit time a 1-9/16 to 2 bit times, in increments of 1/16 bit, can be programmed for character lengths of 6, 7 and 8 bits. For a 5-bit character, the stop bit duration can be programmed from 1-1/16 to 2 bit times.

If an external 1x clock is programmed for the transmitter, MR2(3) = 0 selects a stop bit duration of one bit time and MR2(3) = 1 selects a duration of two bit times for transmission.

The receiver only checks for mark condition at the center of the first stop bit (that is, one bit time after the last data or parity bit is sampled) regardless of the programmed transmitted stop bit length.

CLOCK SELECT REGISTER (Channels A-D)

CSR (7:4) and CSR (3:0) of each channel operate in conjunction with ACR(7) and the channel's set/clear BRG select extend' commands to allow independent selection of the bit rates for the receiver and transmitter respectively. The BRG can generate 33 different bit rates, of which 22 is selected by programming ACR(7). The bit rates generated when using a 3.6864 MHz crystal or an external clock of the same frequency are shown in Table 3A, where 'X' refers to the current state of the extend bit (see CR [7:4] selection). Note that the actual outputs from the BRG are at 16x the bit rates shown in the table.

COMMAND REGISTER (Channels A-D)

Each channel of the QUART has a command register used to supply commands to the respective channel. Multiple commands may be invoked simultaneously by a single write to the command register as long as the commands are non-conflicting.

CR(7:4) - Miscellaneous Commands

The encoded value of this field specifies a single command as follows:

0 0 0 0 - Null Command.

0 0 0 1 - Reset MR Pointer - causes the channel's MR pointer to point to MR1.

0 0 1 0 - Reset Receiver - reset the receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.

0 0 1 1 - Reset Transmitter - resets the transmitter as if a hardware reset had been applied. The TXD output is forced to a high level.

0 1 0 0 - Reset Error Status - clears the received break (RB), parity error (PE), framing error (FE) and overrun error (OE) status bits, SR(7:3). Used in character mode to clear the OE status bit (although the RB, PE, and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.

0 1 0 1 - Reset Break Change Interrupt - clears the channel's break change interrupt status bit.

TABLE 3A CSR [7:4] / [3:0] Bit Rate Selection (3.686 MHz)

Field CSR[7:4] CSR[3:0]	Bit Rate			
	ACR[7] = 0		ACR[7] = 1	
	X = 0	X = 1	X = 0	X = 1
0 0 0 0	50	75	75	50
0 0 0 1	110	110	110	110
0 0 1 0	134.5	134.5	134.5	134.5
0 0 1 1	200	150	150	200
0 1 0 0	300	3600	300	3600
0 1 0 1	600	14.4K	600	14.4K
0 1 1 0	1200	28.8K	1200	28.8K
0 1 1 1	1050	57.6K	2000	57.6K
1 0 0 0	2400	115.2K	2400	115.2K
1 0 0 1	4800	4800	4800	4800
1 0 1 0	7200	1800	1800	7200
1 0 1 1	9600	9600	9600	9600
1 1 0 0	38.4K	19.2K	19.2K	38.4K
1 1 0 1	Timer	Timer	Timer	Timer
1 1 1 0	EXT - 16x	EXT - 16x	EXT - 16x	EXT - 16x
1 1 1 1	EXT - 1x	EXT - 1x	EXT - 1x	EXT - 1x

TABLE 3B CSR [7:4] / [3:0] Bit Rate Selection (7.3728 MHz)

Field CSR[7:4] CSR[3:0]	Bit Rate			
	ACR[7] = 0		ACR[7] = 1	
	X = 0	X = 1	X = 0	X = 1
0 0 0 0	100	150	150	100
0 0 0 1	220	220	220	220
0 0 1 0	269	269	269	269
0 0 1 1	400	300	300	400
0 1 0 0	600	7200	600	7200
0 1 0 1	1200	28.8K	1200	28.8K
0 1 1 0	2400	57.6K	2400	57.6K
0 1 1 1	2100	115.2K	4000	115.2K
1 0 0 0	4800	230.4K	4800	230.4K
1 0 0 1	9600	9600	9600	9600
1 0 1 0	14.4K	3600	3600	14.4K
1 0 1 1	19.2K	19.2K	19.2K	19.2K
1 1 0 0	76.8K	38.4K	38.4K	76.8K
1 1 0 1	Timer	Timer	Timer	Timer
1 1 1 0	EXT - 16x	EXT - 16x	EXT - 16x	EXT - 16x
1 1 1 1	EXT - 1x	EXT - 1x	EXT - 1x	EXT - 1x

0 1 1 0 - Start Break - forces the TXD output low. The transmitter must be enabled to start a break. If the transmitter is empty, the start of the break may be delayed up to two bit times. If the transmitter is active, the break begins when the transmission of that character in the THR is completed, viz., TXEMT must be true before the break will begin.

0 1 1 1 - Stop Break - the TXD line will go high within two bit times. TXD will remain high for one bit time before the next character, if any, is transmitted.

1 0 0 0 - Set Rx BRG Select Extend Bit - sets the receiver BRG select extend bit for the channel to 1.

1 0 0 1 - Clear Rx BRG Select Extend Bit - clears the receiver BRG select extend bit for the channel to 0.

1 0 1 0 - Set Tx BRG Select Extended Bit - sets the transmitter BRG select extend bit for the channel to 1.

1 0 1 1 - Clear Tx BRG Select Extend Bit - clears the transmitter BRG select extend bit for the channel to 0.

1 1 0 0 - Set Standby Mode (Channel A) Reset IUS Latch (Channel B) and Select Direct Systems Clock (Channel C) - when this command is invoked via the channel A command register, power is removed from the transmitters, receivers, counter/timer and additional circuits to place the QUART in the standby mode. Normal operation is restored by a hardware reset or by invoking the 'set active mode' command.

When this command is invoked via the channel B command register, and the QUART (88 Mode) is operating in Z-mode, it causes the interrupt-under-service latch to be reset.

When this command is invoked via the channel C command register, the QUART will generate its internal system clock and take a direct crystal or TTL clock signal to generate a set of standard baud rates described in Table 3A.

1 1 0 1 - Set Active Mode (Channel A) Set Z-mode (Channel B) and Select Divided System Clock (Channel C) - when this command is invoked via the channel A command register the QUART is removed from the stand-by mode and resumes normal operation.

When this command is invoked via the channel B command register, the QUART is conditioned to operate in the Z-mode. This applies only in the 88 mode.

When this command is invoked via the channel C command register, the QUART is set to generate internal system clock after dividing the external clock input frequency by two. In this mode an external 7.3728 MHz clock may be used.

1 1 1 0 - Set Special MR Pointer - this single command, invoked through channel A of the QUART, sets a special pointer which points to all 4 shadow mode registers simultaneously.

1 1 1 1 - Reset Special MR Pointer - this command resets the special mode register pointer and enables access to the normal mode registers.

Note: When writing 'O4H' at the mode register address of the selected channel, this value is written into the selected shadow mode register since the normal mode register address are disabled by the special pointer. In this step the TXFIFO mode bit (bit 2) is set. This procedure can be executed regardless of the state of the normal mode register pointer whose value stays intact throughout the procedure. Note also that the TXFIFO can be activated independently for each channel of the QUART. The lowest two bits (bits 0 and 1) of the shadow mode register are reserved for factory testing and must never be set to 1's.

CR[3] - Disable Transmitter

This command terminates operation of the channel's transmitter and resets the TXRDY and TXEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before going into the inactive state.

CR[2] - Enable Transmitter

This command enables operation of the channel's transmitter and asserts the TXRDY status bit.

CR[1] - Disable Receiver

This command immediately terminates operation of the channel's receiver. Any character being received will be lost. The command has no effect on the receiver status bits or on any other control registers. If the multidrop mode is programmed, the receiver operates even if it is disabled. See OPERATION section.

CR[0] - Enable Receiver

This command enables operation of the receiver. If not in the multidrop mode, it also forces the receiver to start searching for the start bit.

STATUS REGISTER (Channels A-D)

SR[7] - Received Break

This bit indicates that an all zero character of the programmed length was received without a stop bit. Only a single FIFO position is occupied when a break is received. Additional transfers into the FIFO are inhibited until the RXD line returns to the marking state for at least half a bit time. This is defined as two successive edges of the internal or external 1 x clock.

When this bit is set, the channel's change in break status bit in the ISR is set. The bit in the ISR is also set when the end of the break condition, as defined above, is detected.

The chip's break detect logic can detect breaks that begin in the middle of a character. However, the break must persist until the end of the next character time in order for it to be detected.

SR[6] - Framing Error

When set, this bit indicates that RXD was low when the stop bit of the character is the FIFO was sampled. The stop bit check is made in the middle of the first stop bit position (one bit time after sampling the last data bit or the parity bit at its midpoint) regardless of the stop bit length programmed.

SR[5] - Parity Error

This bit is set when the 'with parity' or 'force parity' modes are programmed if the corresponding character in the data FIFO was received with incorrect parity.

In the multidrop mode, this status bit indicates the state of received address/data (A/D) flag bit.

SR[4] - Overrun Error

If set, this bit indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its error status) is overwritten.

This bit is cleared by a 'reset error status' command.

TABLE 5. BIT RATE GENERATOR CHARACTERISTICS
Crystal or Clock Input = 3.6864 MHz or 7.3728 MHz

Nominal Rate (bps)	Actual Clock (KHz)	Error (Percent)
50	0.8	0
75	1.2	0
110	1.759	-0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	-0.26
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
3600	57.6	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
14.4K	230.4	0
19.2K	307.2	0
28.8K	460.8	0
38.4K	614.4	0
57.6	921.6	0
115.2K	1843.2	0

TABLE 6. ACR [6:4] FIELD DEFINITIONS

ACR [6:4]	Mode	Clock Source
0 0 0	Counter	External - IP2/10 Input
0 0 1	Counter	TXCA/C 1x Clock of Channel A/CTx
0 1 0	Counter	TXCB/D 1x Clock of Channel B/DTx
0 1 1	Counter	X1/CLK Input Divided by 16
1 0 0	Timer	External - IP2/10 Input
1 0 1	Timer	External Divided by 16 - IP2/10 Input
1 1 0	Timer	X1/CLK Input
1 1 1	Timer	X1/CLK Input Divided by 16

SR[3] - Transmitter Empty (TXEMT)

This bit is set when the transmitter underruns. It is set after transmission of the last stop bit of a character, if there is no character, the THR is awaiting transmission. It is reset when the THR is loaded by the CPU and when the transmitter is disabled.

SR[2] - Transmitter Ready (TXRDY)

This bit, when set, indicates that the THR is empty and ready to accept a character. The bit is cleared when the THR is loaded by the CPU and is set when that character is transferred to the transmit shift register. TXRDY is set when the transmitter is initially enabled and is reset when the transmitter is disabled. Characters loaded into the THR while the transmitter is disabled will not be transmitted.

SR[1] - FIFO Full (FFULL)

This bit is set when a character is transferred from the receive shift register to the FIFO and the transfer causes it to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

SR[0] - Receiver Ready (RXRDY)

This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when a character is transferred from the receive shift register to the FIFO and reset when the CPU reads the last character currently stored in the FIFO.

OUTPUT PORT CONFIGURATION REGISTER (1, 2)

This register programs the output port to provide alternate functions. Note that when an output is programmed as an interrupt, it is not masked by the contents of the IMR.

OPCR [7/15] - OP7/OP15 Output Select

This bit programs the OP7/OP15 output to provide one of the following:

0 - The complement of OPR[7]/[15].

1 - The channel B/D transmitter interrupt TXRDY B/D which is the complement of SRB/D [2]. In this mode, OP7, and/or OP15 are open drain outputs.

OPCR [6/14] - OP6/OP14 Output Select

This bit programs the OP6/OP14 output to provide one of the following:

0 - The complement of OPR[6]/[14].

1 - The channel A/C transmitter interrupt output, TXRDY A/C which is the complement of SRA/C[2]. In this mode OP6/OP14 are open drain outputs.

OPCR [5/13] - OP5/OP13 Output Select

This bit programs the OP5/OP13 output to provide one of the following:

0 - The complement of OPR[5]/[13].

1 - The channel B/D receiver interrupt output, which is the complement of ISR[5]. In this mode OP5/OP13 are open drain outputs.

OPCR [4/12] - OP4/OP12 Output Select

This bit programs the OP4/OP12 output to provide one of the following:

0 - The complement of OPR[4]/ [12].

1- The channel A/C receiver interrupt output, which is the complement of ISR[5]. In this mode OP5/OP12 are open drain outputs.

OPCR[3:2] - OP3/OP12 Output Select

These bits program the OP3/OP11 output to provide one of the following:

00 - The complement of OPR[3]/[11].

01 - The counter/timer output, in which case OP3/OP11 is an open drain output. In the timer mode the output is a square wave at the programmed frequency. In counter mode the output remains high until the terminal count is reached, at which time it goes low. The output returns to the high state when the counter is stopped by a stop counter command.

10 - The 1x clock which shifts the output data for the channel B/D transmitter. A free running 1x clock is output if data is not being transmitted.

11 - The 1x clock which samples the input data for the channel B/D receiver. A free running 1x clock is output if data is not being received.

OPCR [1:0] - OP2/OP10 Output Select

These bits program the OP2/OP10 output to provide one of the following:

00 - The complement of OPR[2]/[10].

01 - The 16x clock selected for the channel A transmitter by CSRA/C[3:0]. This will be a 1x clock if external 1x clock is programmed.

10 - The 1x clock which shifts the output data for the channel A/C transmitter. A free running 1x clock is output if data is not being transmitted.

11 - The 1x clock which samples the input data for the channel A/C receiver. A free running clock is output if data is not being received.

AUXILIARY CONTROL REGISTER (1,2)

ACR[7] - Bit Rate Set Select

This bit selects one of two bit rates to be generated by the BRG. The bit rates provided are selected by the channel A through D receiver and transmitter as described in the Clock Select Register description. Bit rate generator characteristics are shown in Table 5.

ACR [6:4] - Counter/Timer Mode and Clock Source Select

This field selects the operating mode and clock source for the counter/timer. See Table 6.

ACR [3:0] - Change of State Interrupt Enables

These bits select which bits of the input port cause the input port change bit in the interrupt status register (ISR[7]) to be set. If one of these bits is 'on', the setting of the corresponding bit in the IPCR by a change of state on the input will set ISR[7], and will also cause the interrupt request pin to be asserted if IMR[7] is set. However, if the bit is 'off', the setting of the corresponding bit in the IPCR has no effect on ISR[7].

INPUT PORT CHANGE REGISTER (1,2)

IPCR [7:4] - IP0 - IP3, IP8 - IP11 Change of State

These bits are set when a change of state occurs at the respective input pins (see Input Port Section). The bits are cleared when the CPU reads the IPCR1,2.

The setting of these bits can be programmed to cause an interrupt to the CPU via ACR[3:0], ISR[7] and IMR[7].

IPCR [3:0] - IP3 - IP0, IP11 - IP8 Current State

These bits indicate the current state of the respective inputs at the time the IPCR is read.

INTERRUPT STATUS REGISTER

This register provides the current status of all possible interrupt conditions. If a bit in the ISR is a '1' and the corresponding bit in the interrupt mask register (IMR) is also a '1' the interrupt request output will be asserted. If the corresponding bit in the IMR is a '0' the state of the bit in the ISR has no effect on the interrupt request output. The contents of this register can be read by the CPU either unmasked or masked by the IMR. See Table 1.

ISR[7] - Input Port Change Status

This bit is a '1' when a change of state has occurred at the IPO - IP3 or IP8 - IP11 inputs and that event has been programmed to cause an interrupt via ACR[3:0]. It is cleared when the CPU reads the IPCR.

ISR[6] - Channel B/D Receiver Ready or FIFO Full

This bit indicates that the channel B or D receiver has detected the beginning or end of a received break. It is reset when the CPU invokes a channel B/D 'reset break change interrupt' command.

ISR[5] - Channel B/D Receiver Ready or FIFO Full

The function of this bit is programmed by MR1B/D[6]. If programmed as receiver ready, it indicates that data is in the FIFO. It is set when a character is transferred from the receive shift register to the FIFO and cleared when the CPU reads the RHR. If there are still more characters in the FIFO after the read operation, the bit will be set again after the FIFO is 'popped.'

If this bit is programmed as FIFO full, it is set when a character is transferred from the receive shift register to the FIFO and the transfer causes the FIFO to become full. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, this bit will be set again after the read operation, when that character is loaded into the FIFO.

ISR[4] - Channel B/D Transmitter Ready

This bit is a duplicate of TXRDYB/D, SRB/D[2]

ISR[3] - Counter Ready

In the counter mode, this bit is set when the counter reaches the terminal count and is reset when the counter is stopped by a 'stop counter' command. The command, however, does not stop the C/T.

ISR[2] - Channel A/C Change In Break

This bit indicates that the channel A/C receiver has detected the beginning or end of a received break. It is reset when the CPU invokes a channel A/C 'reset break change interrupt' command.

ISR[1] - Channel A/C Receiver Ready or FIFO Full

The function of this bit is programmed by MR1A/C[6]. If programmed as receiver ready, it indicates that data is in the FIFO. It is set when a character is transferred from the receive shift register to the FIFO and cleared when the CPU reads the RHR. If there are still more characters in the FIFO after the read operation, the bit

will be set again after the FIFO is 'popped.'

If this bit is programmed as FIFO full, it is set when a character is transferred from the receive shift register to the FIFO and the transfer causes the FIFO to become full. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, this bit will be set again after the read operation, when that character is loaded into the FIFO.

ISR[0] - Channel A/C Transmitter Ready

This bit is a duplicate of TXRDYA/C, SRA/C(2).

INTERRUPT MASK REGISTER (1,2)

This register selects which bits in the ISR cause an interrupt to be asserted. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the interrupt request output will be asserted. If the corresponding bit in the IMR is a '0', the state of the bit in the ISR has no effect on the interrupt request output. Note that the IMR does not mask the programmable interrupt outputs, OP3-OP7 and OP11-OP15.

COUNTER/TIMER REGISTERS (CTUR/CTLR)

The CTUR and CTLR hold the eight MSBs and eight LSBs respectively of the value to be used in the counter/timer in both of its modes of operation. The minimum value which may be loaded into CTUR/CTLR is 0001H. These registers are write-only and cannot be read by the CPU.

INTERRUPT VECTOR REGISTER (1,2)

The IVR holds the value which the QUART places on the data bus in response to assertion of the interrupt acknowledge input. In the 88 mode the register is not used for any function when the device operates in I-mode but remains writable and readable by the CPU, and can be used for any purpose. The contents of this register are initialized to OFH by a hardware reset.

The following is a list of features which have been modified or enhanced over the DUART.

1). IEI, IEO and IACK are separate pins, no longer shared with IP4, IP5 and IP6.

2). Address A4/A5 has been added to provide additional internal registers.

3). Two additional inputs have been provided IP7 and IP15.

4). Reset input is debounced for Min of 20 n sec (Min).

5). The QUART is designed to operate with 7.3728 MHz crystal or an external TTL level clock.

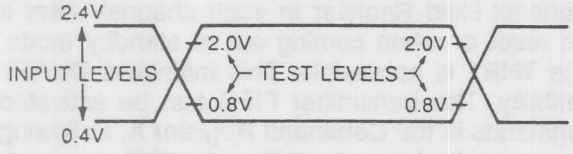
6). Buffered system clock is provided to drive additional external logics (bonding option).

7). Since the interrupt is prioritized, channel A has highest priority and channel D has lowest priority. This determines the order of interrupt vector response on interrupt acknowledge cycles.

8). The QUART has a three byte FIFO stack behind the Transmit Hold Register in each channel. After a system reset or when coming out of standby mode, only the THR1 is accessible. This maintains DUART compatibility. The transmitter FIFO can be activated via commands in the Command Register A. Following steps are required to set additional FIFO's for each transmitter. Each channel in the QUART contains a shadow mode register, writing "E0" in the command register A will enable the shadow mode registers (A - D). Writing "04" in each channel will enable the additional FIFO registers, by writing "F0" in the command register A will exit the shadow mode.

NOTES:

1. Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the Electrical Characteristics section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltage larger than the rated maxima.
3. Parameters are valid over the specified temperature and operating supply ranges. Typical values are at 25°C, V_{CC} = 5V and typical processing parameters.
4. All voltages are referenced to ground (GND). For testing, input signal levels are 0.4V and2.4V with a transition time of 20ns maximum. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate. See Figure 3.
5. Measured operation with a OR7.3MHz crystal and with all outputs open.
6. AC test condition for outputs: C_L = 50pF, R_L = 2.7K ohm to V_{CC}.
7. For the 88 mode, timing is illustrated and referenced to the RDN and WRN inputs. The device may also be operated using CEN as the 'strobing' input. In this case, all specifications apply referenced to the falling and rising edges of CEN.
8. If CEN is used as the strobing input, this parameter defines the minimum high time between CENs.
9. Consecutive write operations to the same register require at least three edges of the X1 clock between writes.
10. This parameter is system dependent. For any QUART in the daisy chain, t_{IAS} must be greater than the sum of t_{EOD} for the highest priority device in the daisy chain, t_{EIS} for the QUART, and t_{DIO} for each device separating them in the daisy chain.
11. This specification imposes a 6MHz maximum 68000 clock frequency if a read or write cycle follows immediately after the previous read or write cycle. A higher 68000 clock can be used if this is not he case.
12. This specification imposes a lower bound on CSN and IACKN low, guaranteeing that they will be low for at least one CLK period.
13. The minimum high time must be at least 1.5 times the X1/CLK period and the minimum low time must be at least equal to the X1/CLK period if either channel's R_X is operation in external 1x clock mode.
14. For prime grade N, P, J, L, M, ML, V_{CC} = 5V±10%.



AC testing inputs are driven at 0.4V for a logic '0' and 2.4V for a logic '1', except for −40 to 85° C and −55 to 125° C, logic '1' shall be 2.6V. Timing measurements are made at 0.8V for a logic '0' and 2.0V for a logic '1'.

Figure 3. Input and Output levels for Timing Measurements

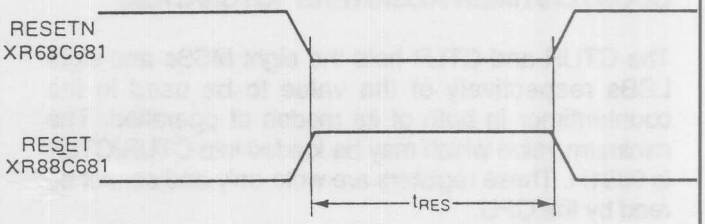


Figure 4. Reset Timing

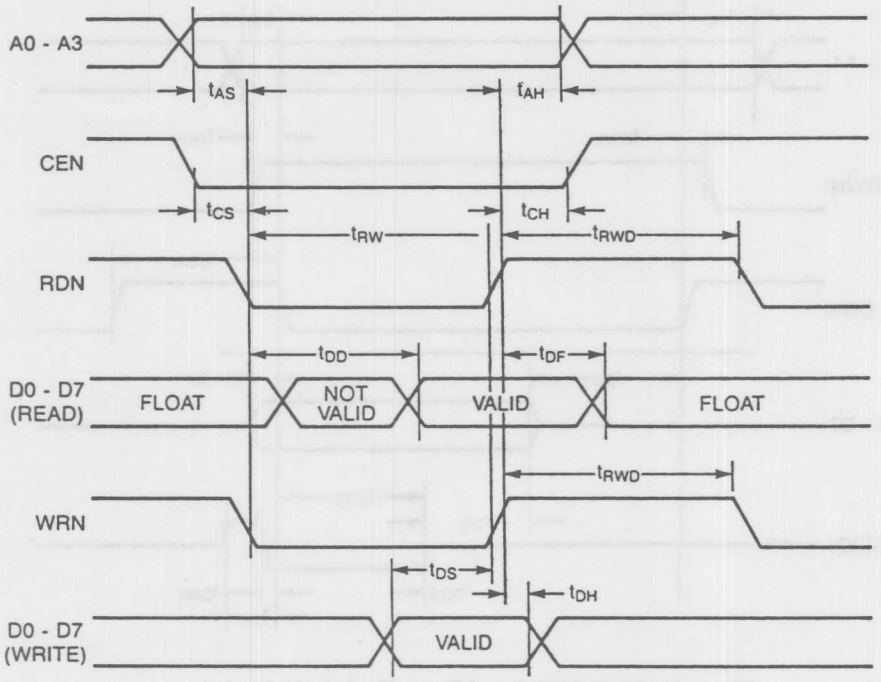


Figure 5. XR 82C684 Read and Write Cycle Timing (88 Mode)

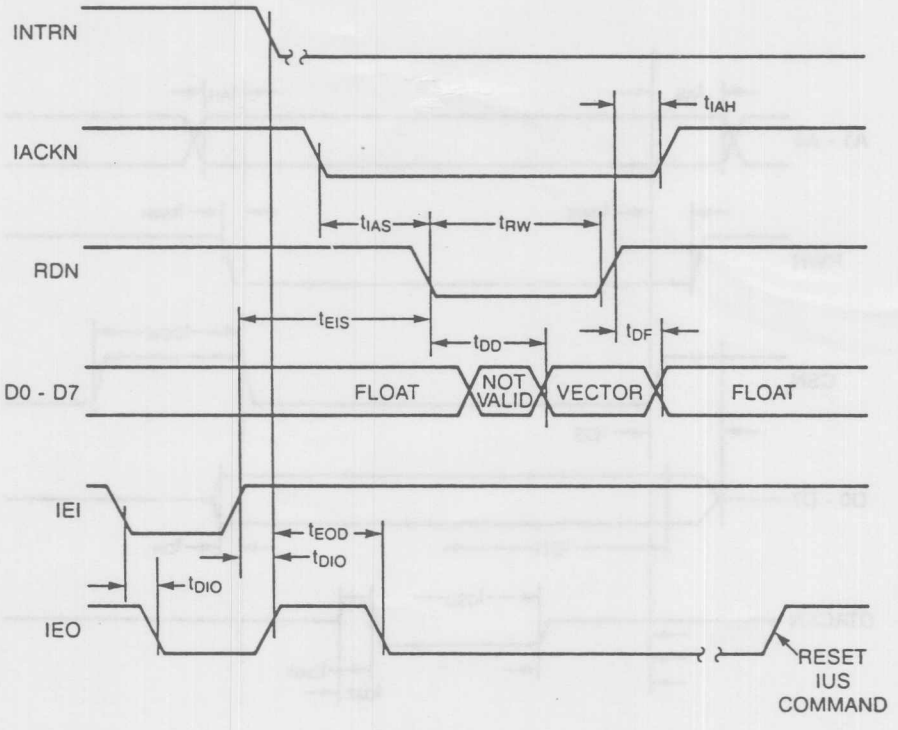


Figure 6. XR 82C684 Z Mode Interrupt Cycle Timing (88Mode)

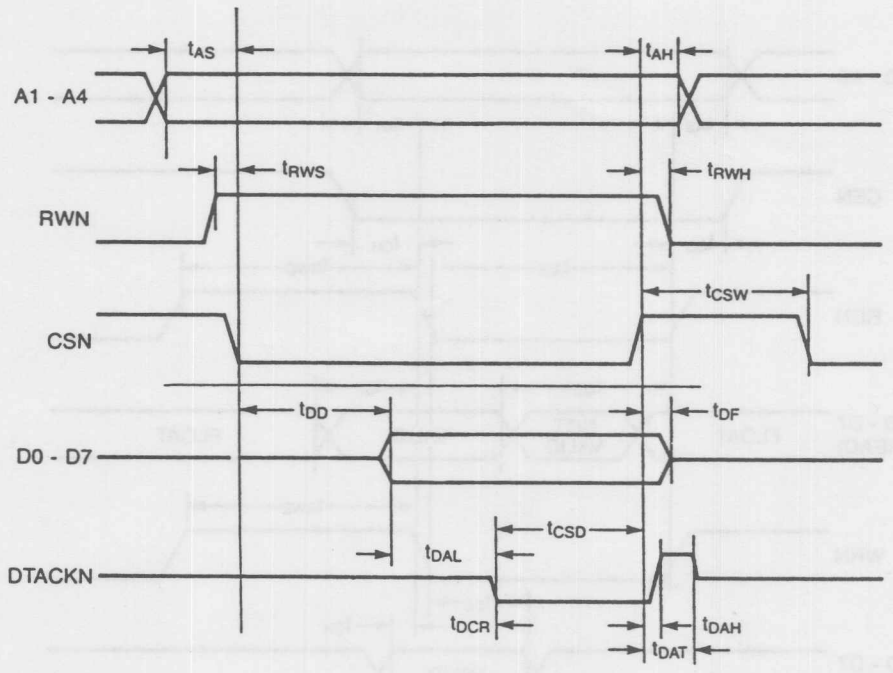


Figure 7. XR 82C684 Read Cycle Timing (68 Mode)

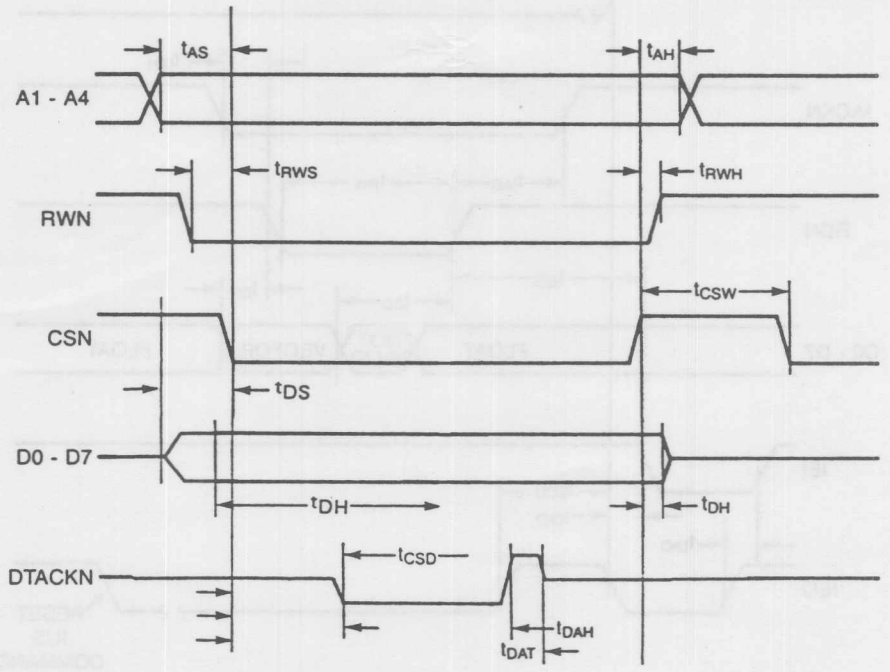


Figure 8. XR 82C684 Write Cycle Timing (68 Mode)

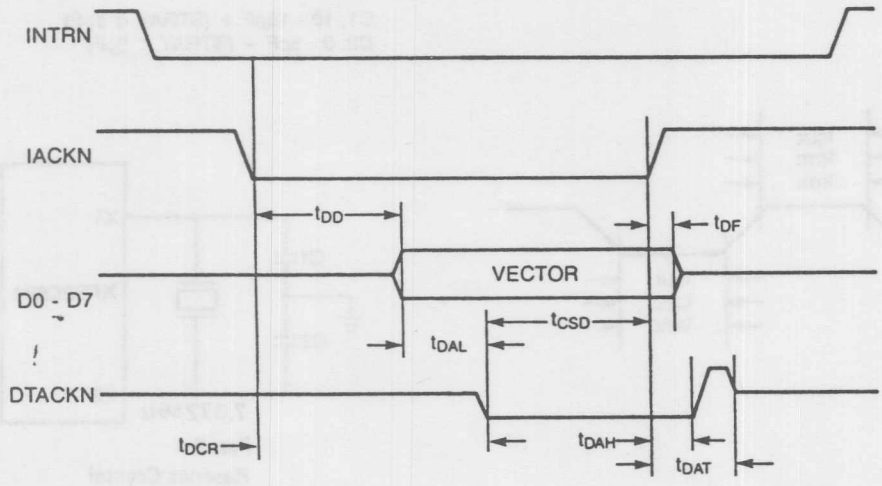


Figure 9. XR 82C684 Interrupt Cycle Timing (68 Mode)

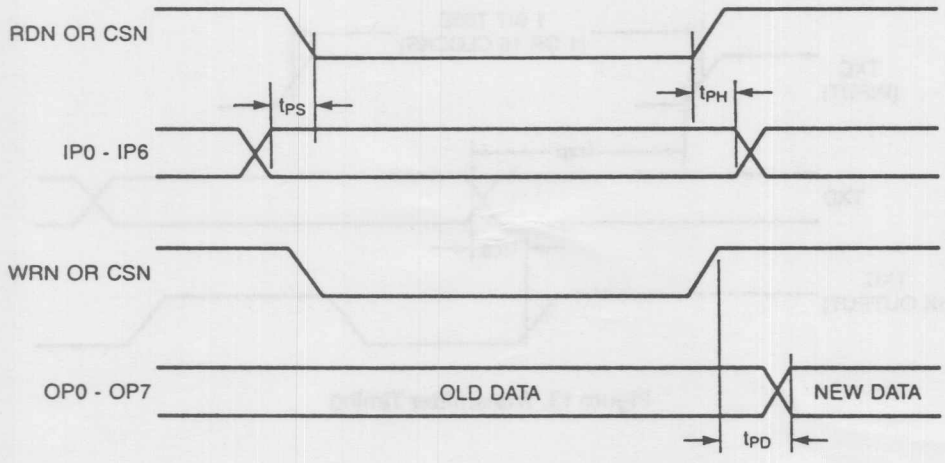
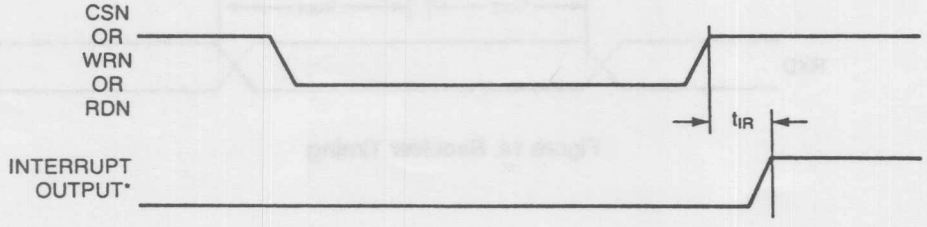


Figure 10. Port Timing



*INTRN or OP3 - OP7 when used as interrupt outputs.

Figure 11. Interrupt Timing

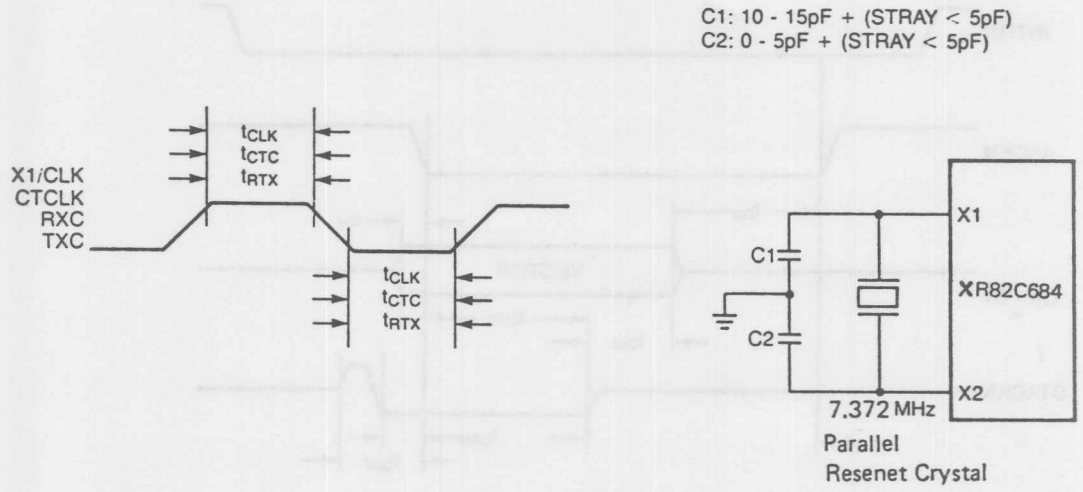


Figure 12. Clock Timing

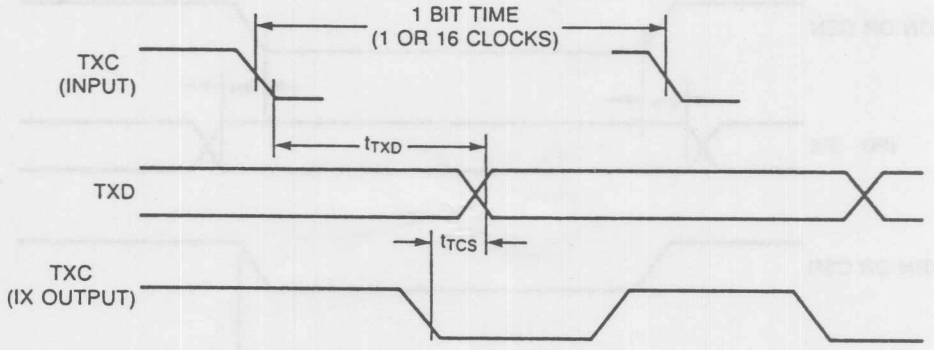


Figure 13. Transmitter Timing

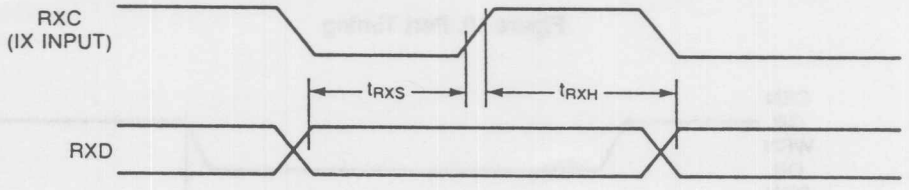
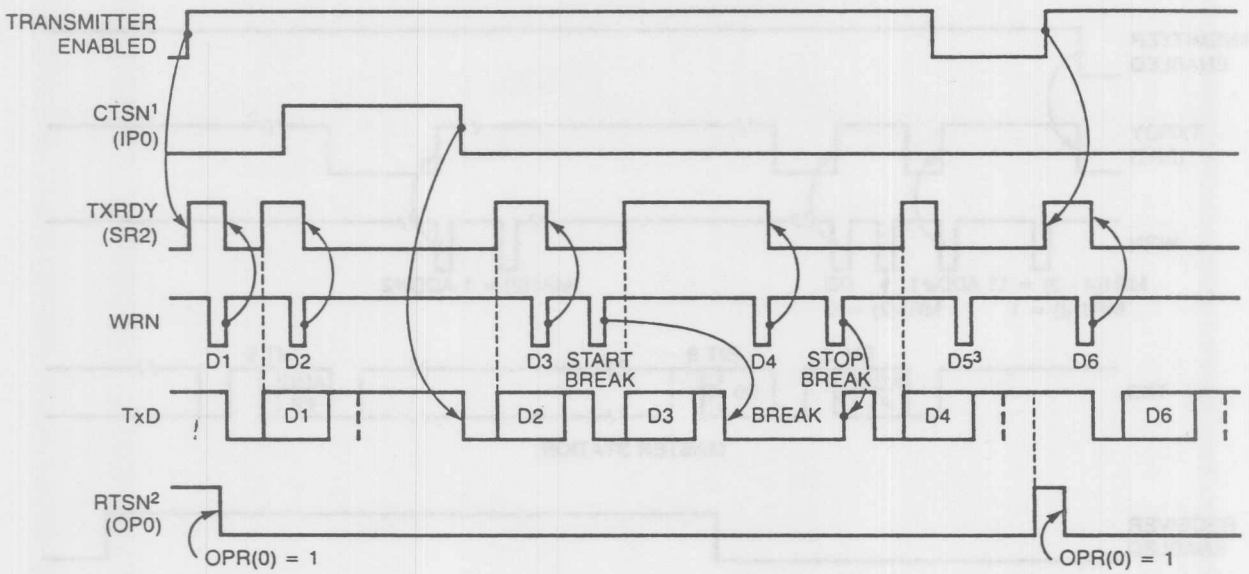
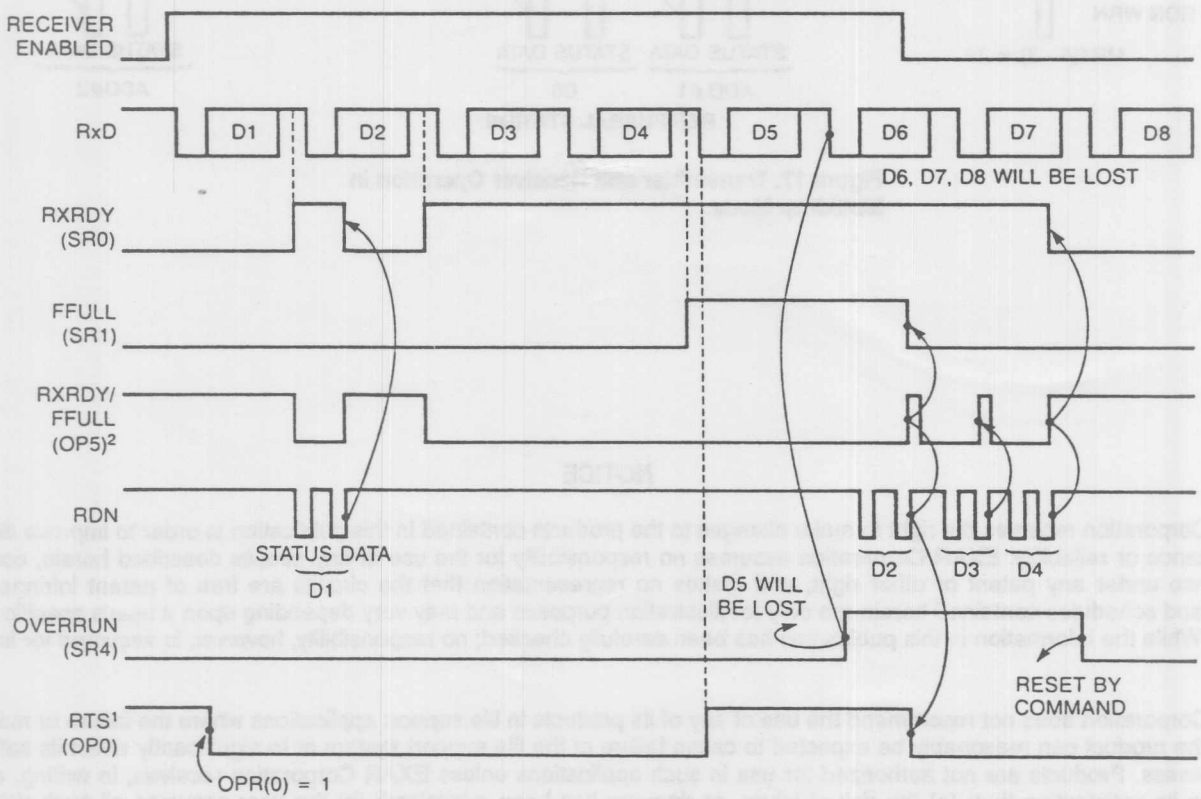


Figure 14. Receiver Timing



NOTES
1. Operation shown for MR2(4) = 1
2. Operation shown for MR2(5) = 1
3. D5 will not be transmitted

Figure 15. Transmitter Operation



NOTES
1. Operation shown for MR1(7) = 1
2. Shown for OPCR(4) = 1 and MR1(6) = 0

Figure 16. Receiver Operation

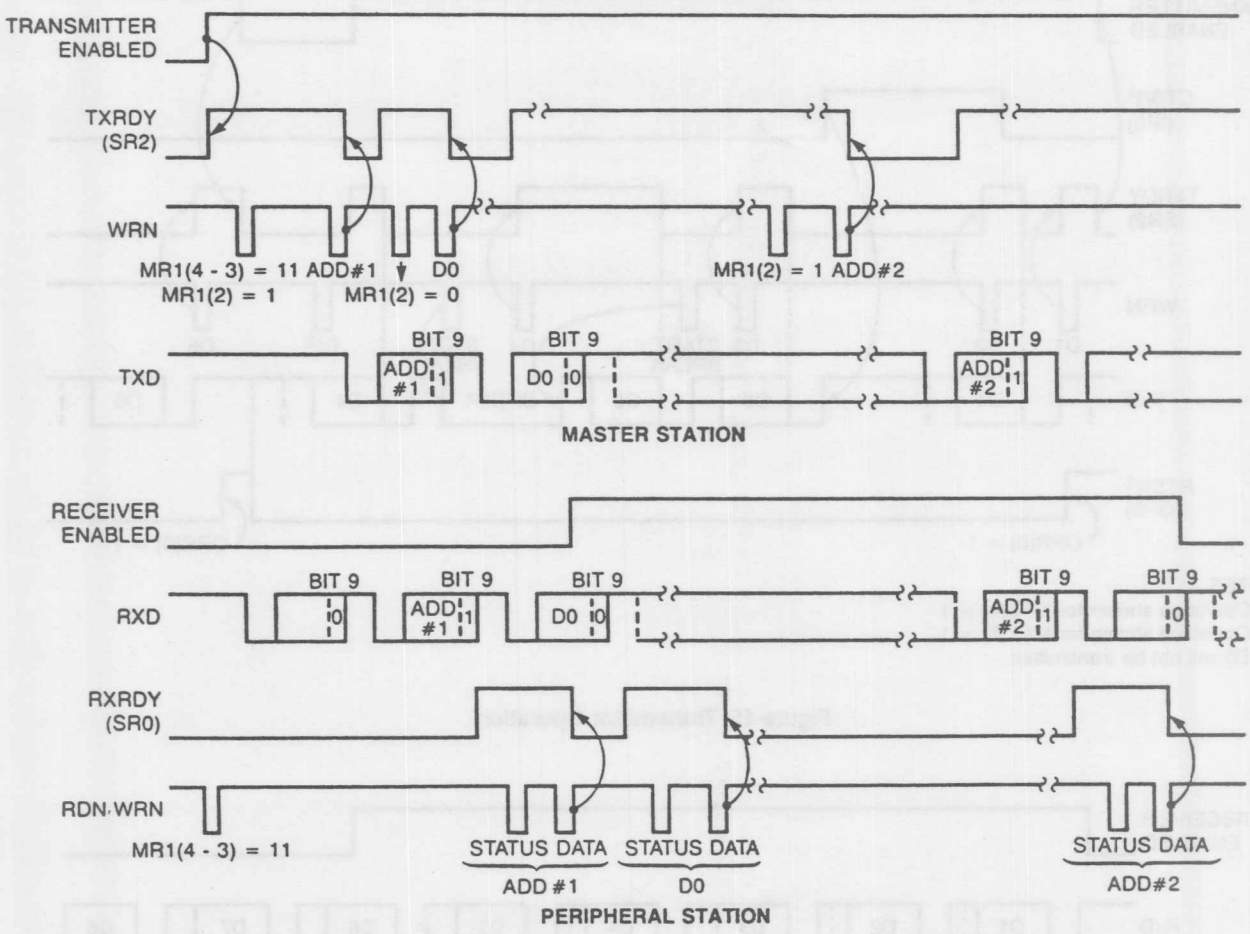


Figure 17. Transmitter and Receiver Operation in Multidrop Mode.

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Data Sheet May 1989